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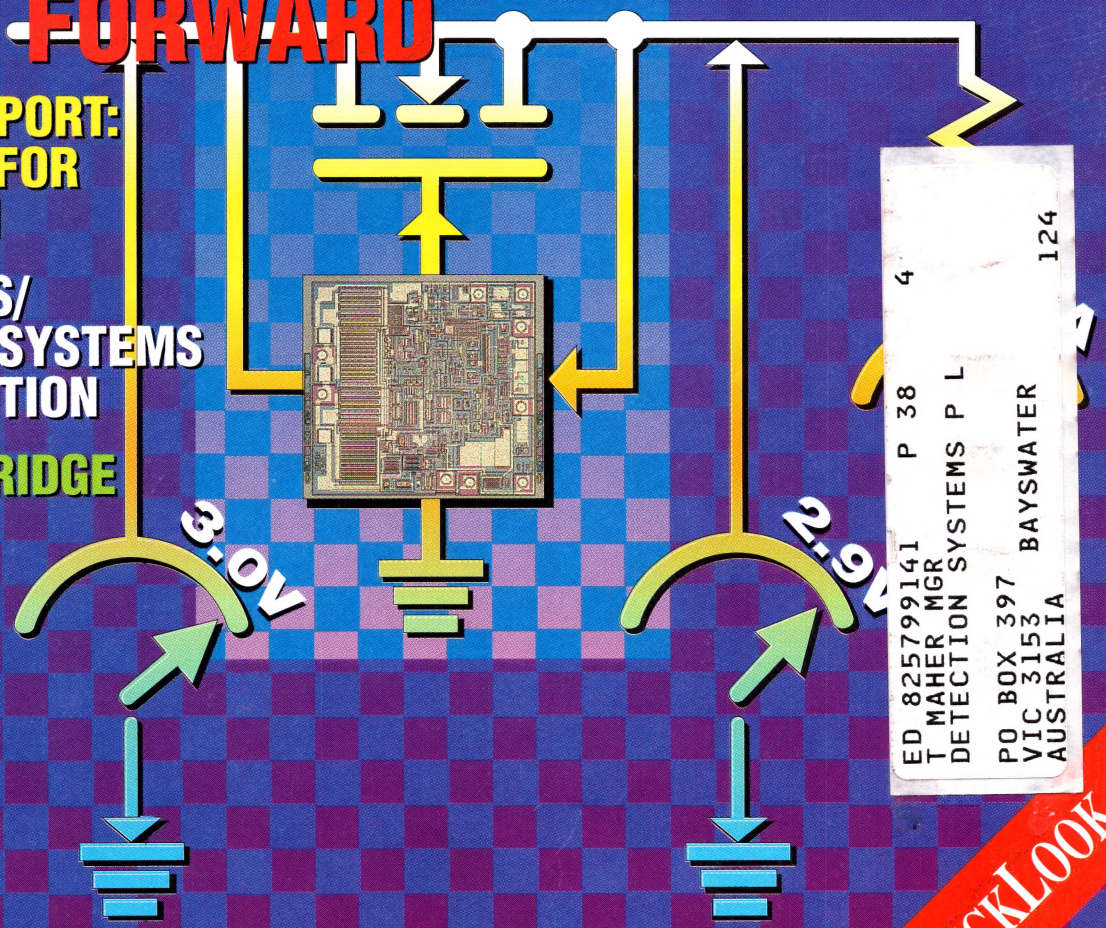
ELECTRONIC DESIGN

MARCH 7, 1994

FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

LOW-DROPOUT REGULATOR TECHNOLOGY TAKES A STEP FORWARD

- SPECIAL REPORT: EDA TOOLS FOR DSP DESIGN
- COMPUTERS/ EMBEDDED SYSTEMS DESIGN SECTION
- PEASE PORRIDGE



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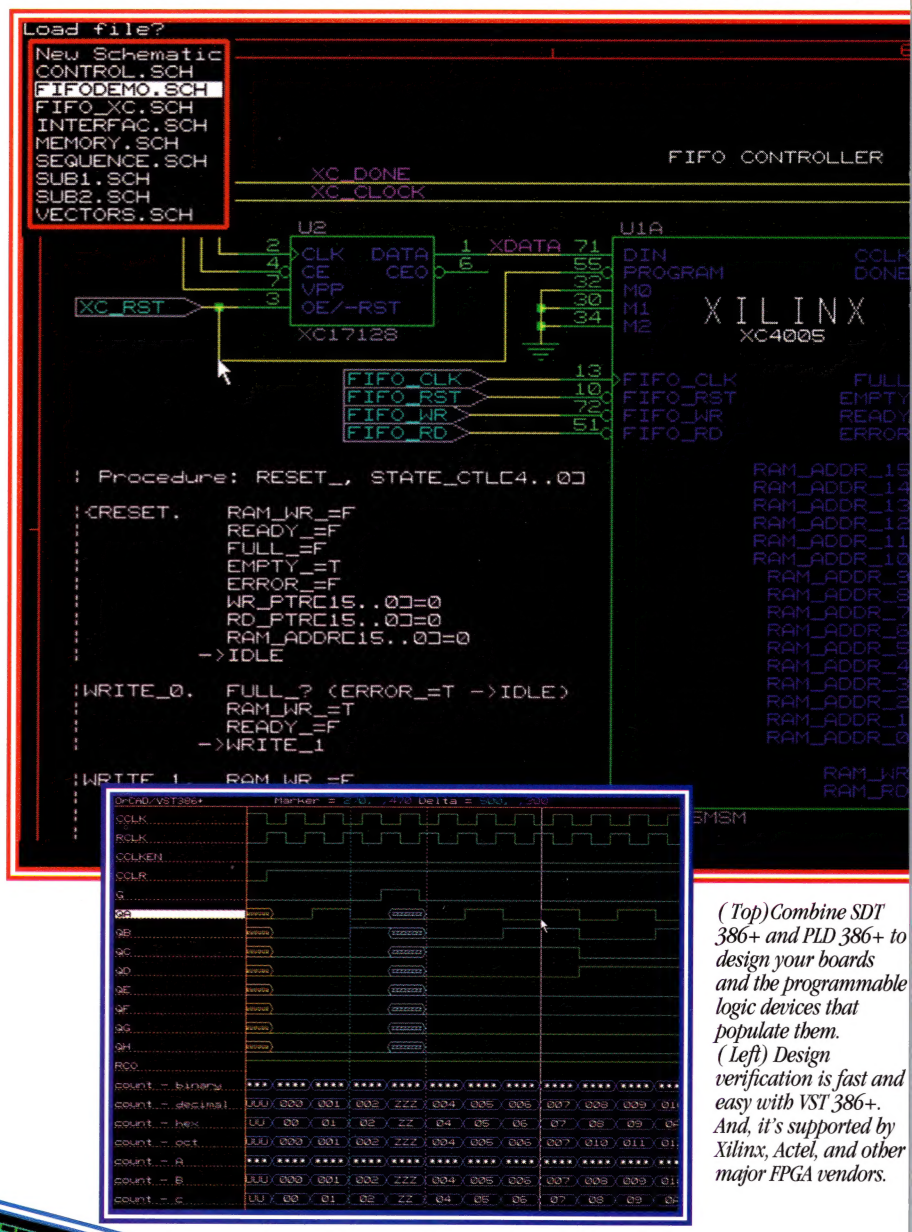

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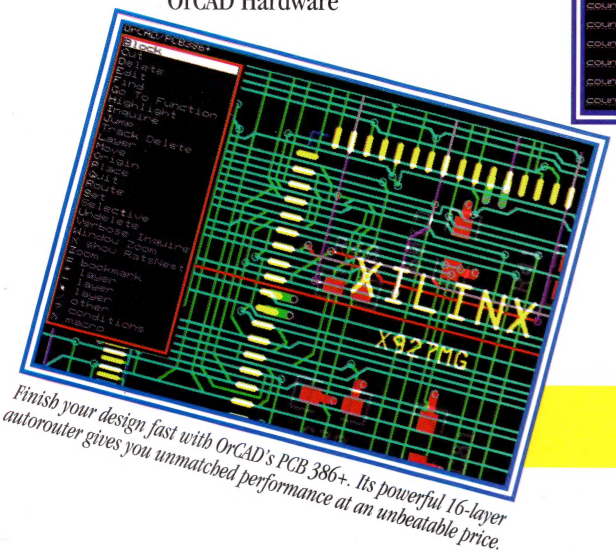

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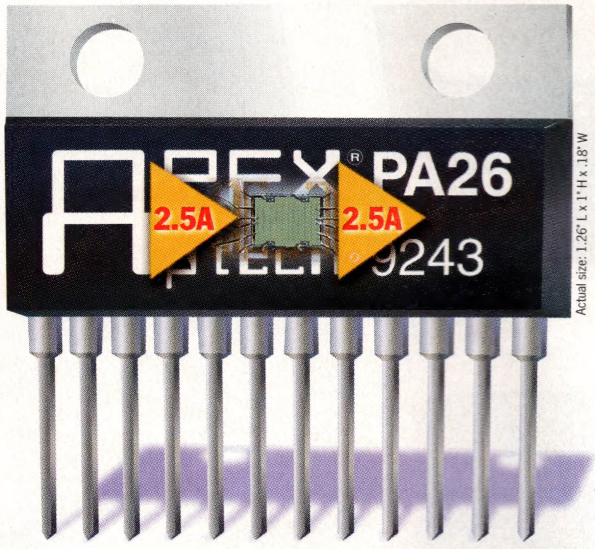

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PA25	5V-40V	2.5A x 2	$-V_S$-.3V	3V @ 2.5A	TO-3[1]	$19.75
PA21	5V-40V	2.5A x 2	$-V_S$-.3V	3V @ 2.5A	TO-3[1]	$23.95
PA21M[2]	5V-40V	2.0A x 2	$-V_S$-.3V	3.5V @ 2A	TO-3[1]	$65.90

[1] The TO-3 is a hermetic package; the SIP is a non-hermetic package
[2] "M" designates hi-rel military grade

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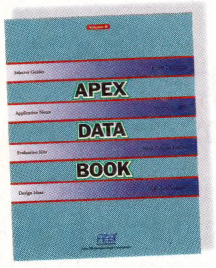

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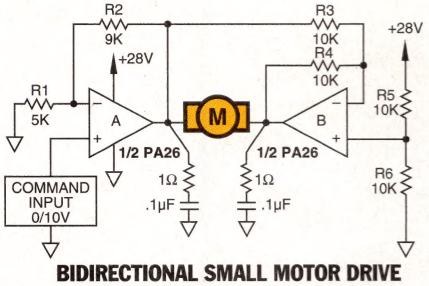
Information on the **PA26**, **PA25** and the **PA21** is included in the new 6th edition *Apex DC/DC Converters, Power and HV Amplifiers* data book. Call today for your free copy. **1-800-862-1021.**



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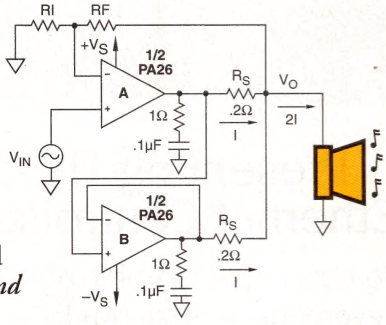

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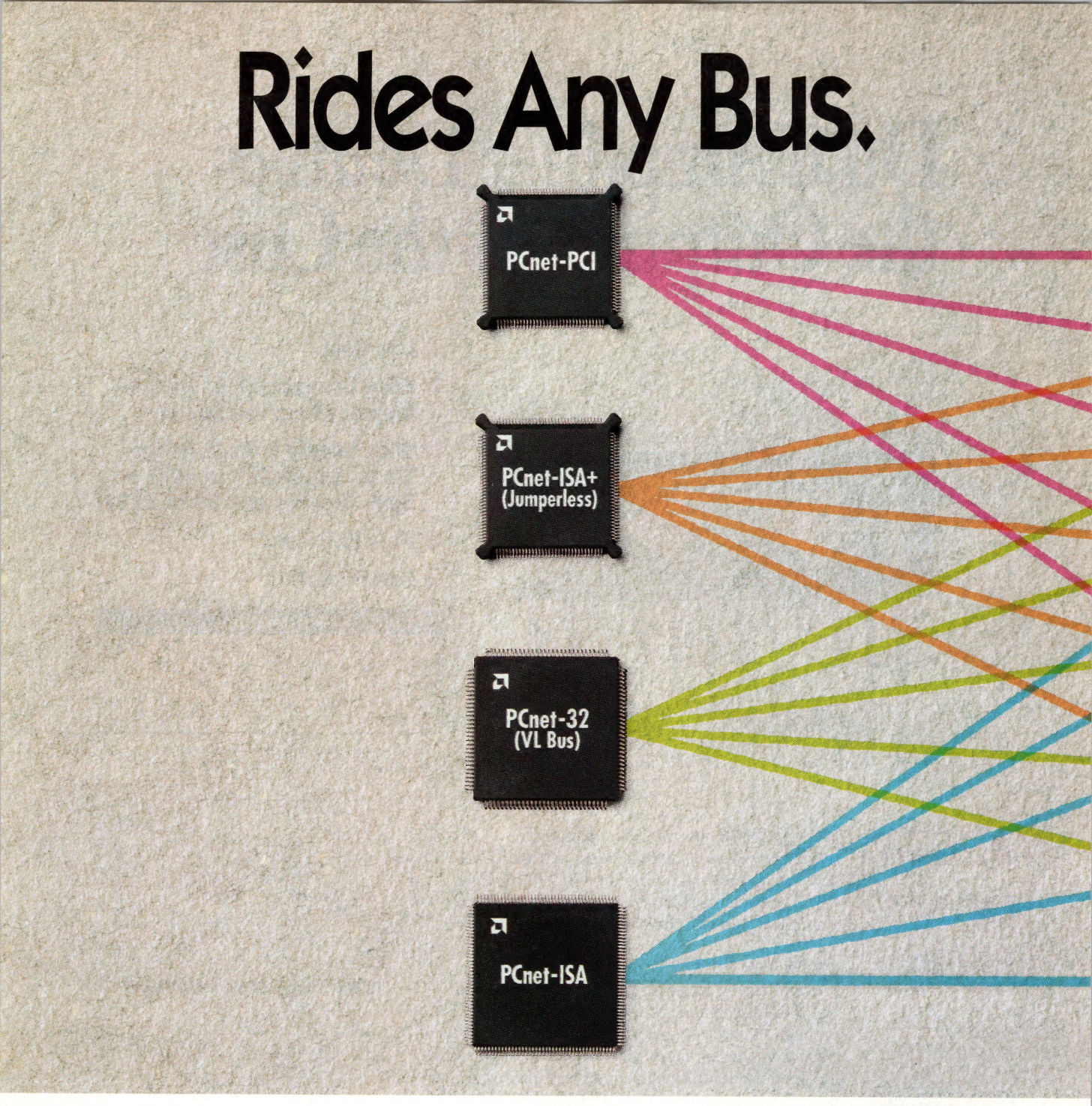

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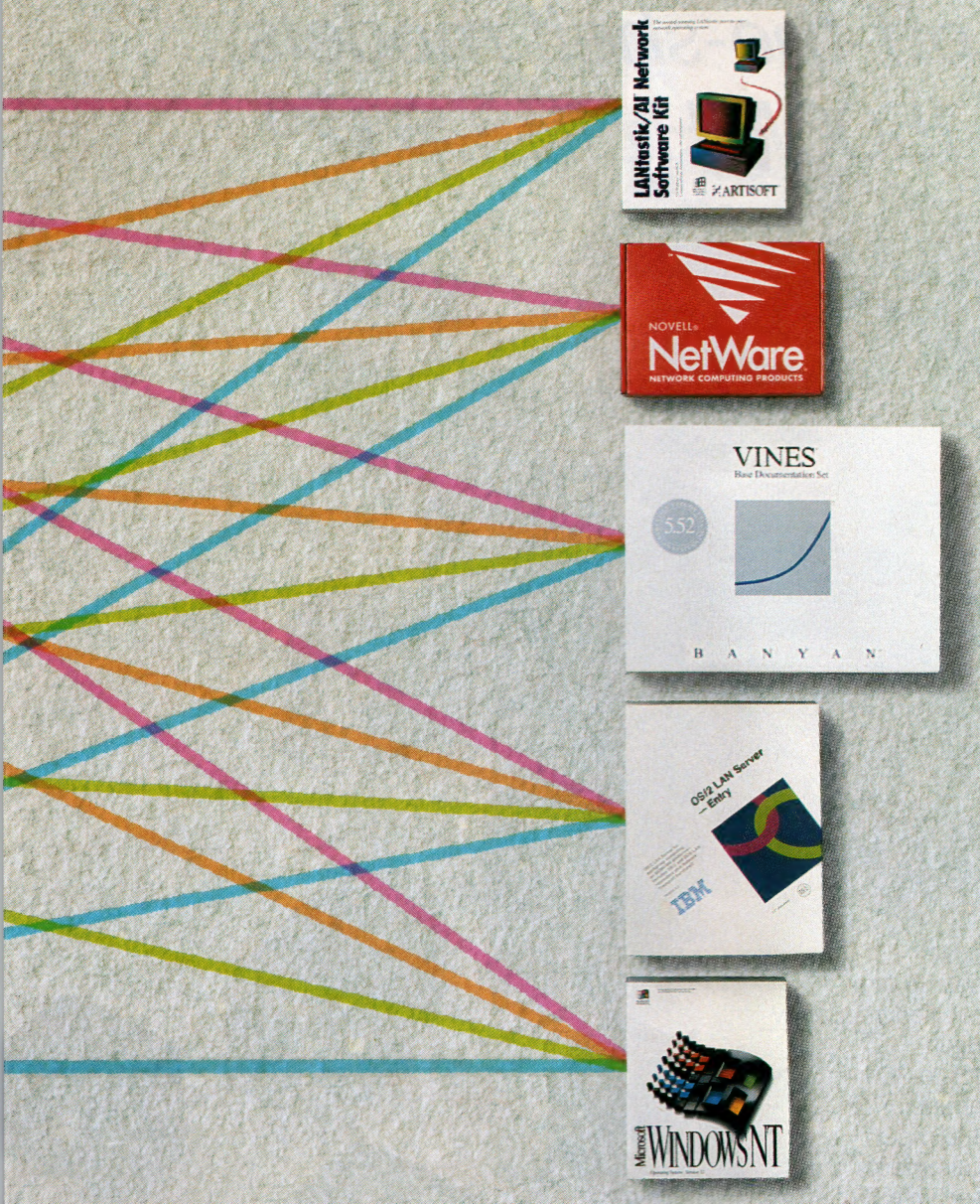

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MARCH 7, 1994 VOL. 42, NO. 5

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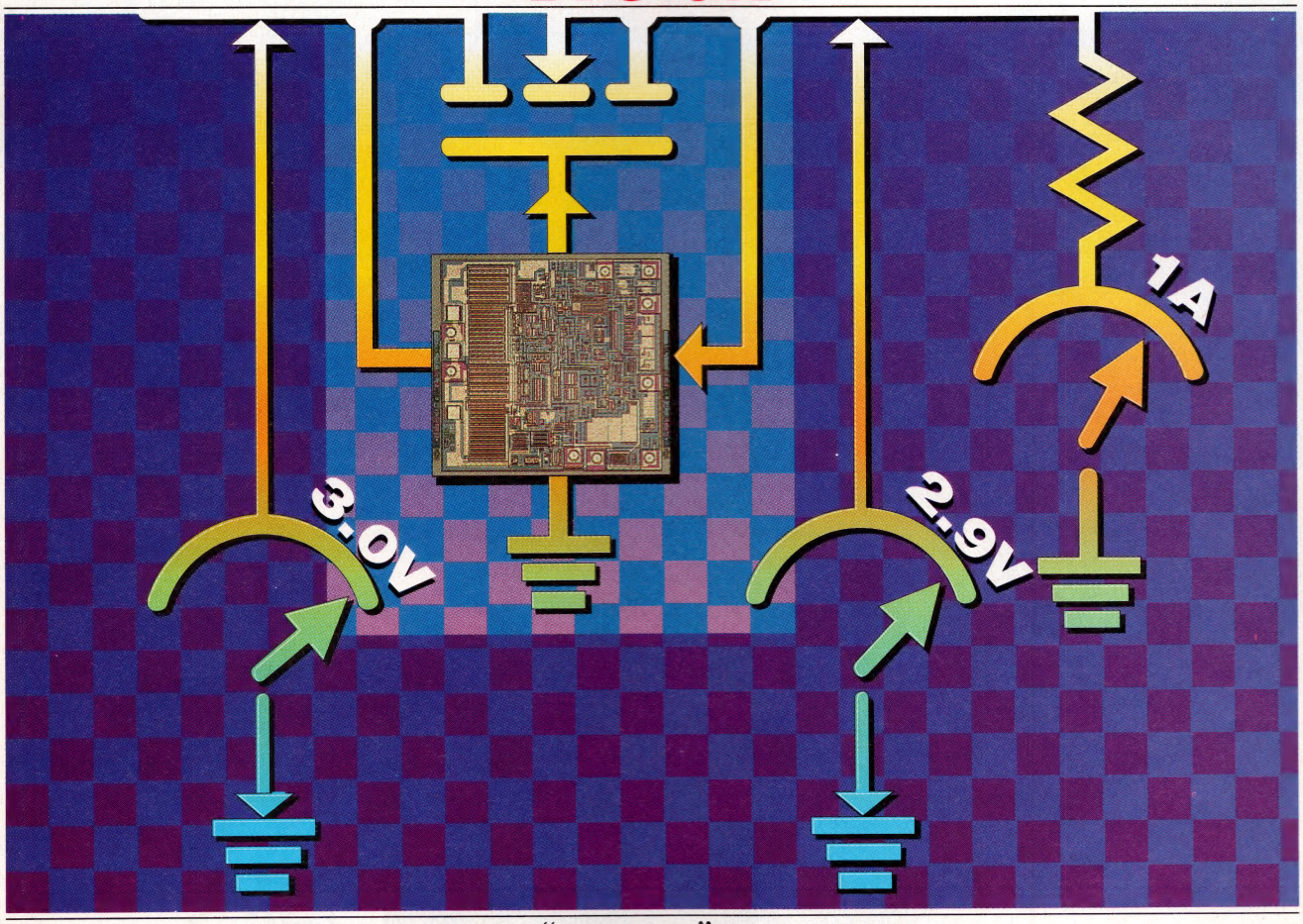

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TINY IC PLUS FET BUILDS "SUPER LDO" REGULATOR . . . 45
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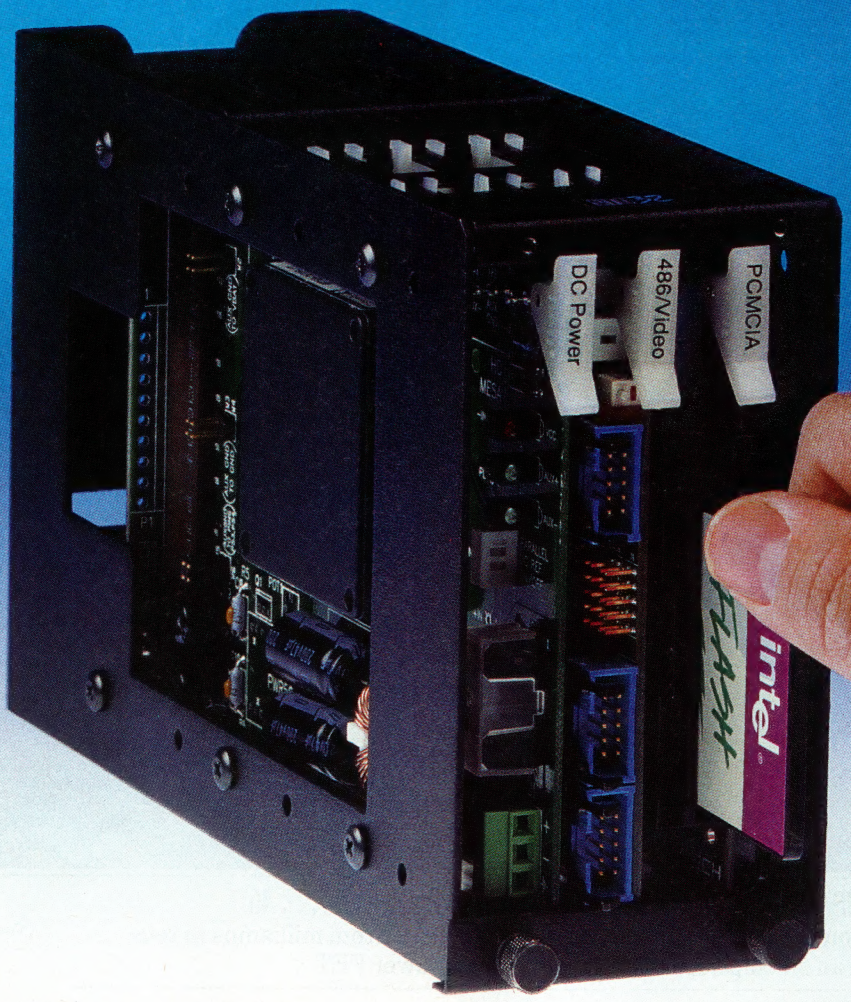
SERIOUS DOWNSIZING

ANOTHER STD 32 INNOVATION



intel inside

SERIOUS SPACE SAVINGS

Ziatech's new microCAT Automation Engine brings big 486 performance to control applications with limited space.

SERIOUS SPECS

While several configurations and options are available, the microCAT pictured above features

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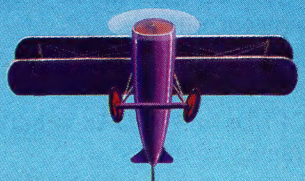

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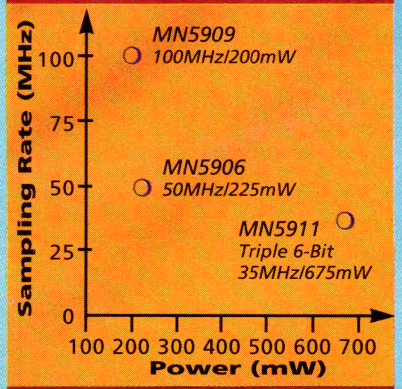

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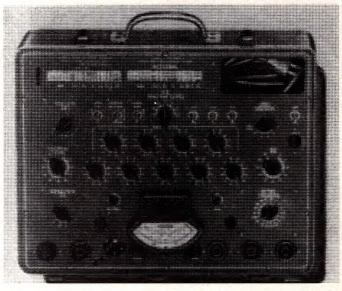
ELECTRONIC DESIGN 40 YEARS AGO

Tube tester: Proportional Gm type

The Model 981 Type 2 Tubechecker provides for the accurate, rapid measurement of proportional mutual conductances, emission characteristics of rectifiers and diodes, and the firing potential limits of voltage regulators and low power thyratrons. A feature is the provision for accurate meter measurement of leakage resistance, as high as 5 Meg, between the tube elements. In addition, the tester measures transconductance up to 24,000 micromhos, in four ranges. Multiple switching permits any combination of tube connections to be made. Three toggle switches make it possible to quickly check and compare the respective sections of twin-section tubes at only one setting of the selector switch. Sockets are provided for all conventional tube type bases as well as acorn, and 7 and 8 pin subminiatures. The instrument also includes a roll chart which places complete tube test data at the user's fingertips. Weston Electrical Instrument Corp., Dept. ED, 614 Frelinghuysen Ave., Newark 5, N.J.



This product will be on display in Booth 533-535 at The Radio Engineering Show. *(Electronic Design, March 1954, p. 31.)*

Here's another tester from the venerable Weston Instrument Corp. of Newark, N.J. The 1954 Radio Engineering Show, where this tester was on display, was held at the Kingsbridge Armory in the Bronx, N.Y., and drew more than 40,000 attendees. It was the forerunner of the IEEE Show, which later became Electro. Attendance for what was considered the major electronics industry event of the year during the '50s and '60s climbed to over 70,000. But it eventually began to decline in importance as well as attendance as other, more specialized shows took root.—SS

Purifying Germanium

Germanium for transistors can now be refined to 99.99999999% purity in a new "zone-melting" process developed by W.G. Pfann of Bell Telephone Laboratories, New York, N.Y. The process is based on the fact that impurities are not equally soluble in the solid and liquid states of a substance. Usually, impurities are more soluble in the liquid. To take advantage of this, a narrow molten zone produced by a circular induction heater is moved slowly along an ingot of relatively impure material to "sweep" the impurities to one end of the ingot. The molten zone tends to hold the impurities while the ingot solidifies into a purer state on the other side of the heater.

A series of circular heaters is used and each molten zone extracts its share of impurities from that left by the preceding zone. At the end of the run, substantially all the impurities have been "swept" to one end of the ingot. They are trapped in the tip of the ingot when it passes out of the heater and solidifies. This tip may then be cut off. The behavior of germanium in transistors is affected critically by the presence of impurities, but the kind and amount of impurities must be rigidly controlled for efficient operation. This is accomplished by refining an ingot of germanium to a near-perfect state of purity by the zone-melting process. Then its electrical properties can be altered to the desired degree by the controlled addition of such impurities as arsenic and antimony.

The process, which has already been adapted to production needs, can also purify other substances such as tin, antimony, and semiconductors. The method is also useful in identifying impurities in materials which cannot be detected by other means.*(Electronic Design, March 1954, p. 5.)*

This modest news item covers one of the most significant developments in the first decade of semiconductor processing. Pfann's zone-refining process was the key to providing the fledgling semiconductor industry with a large supply of ultra-high-purity single-crystal germanium.—SS

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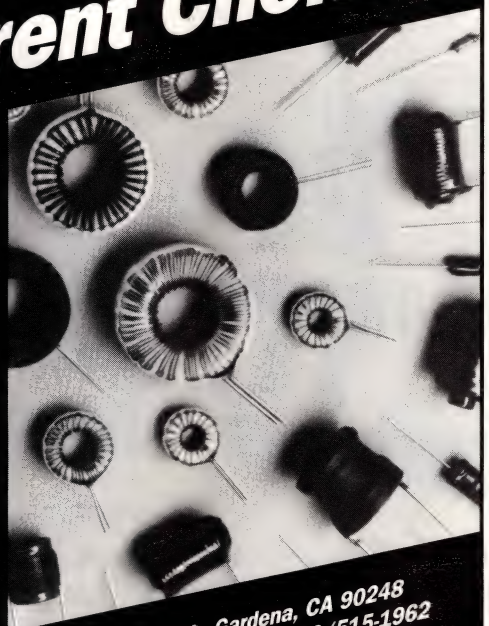

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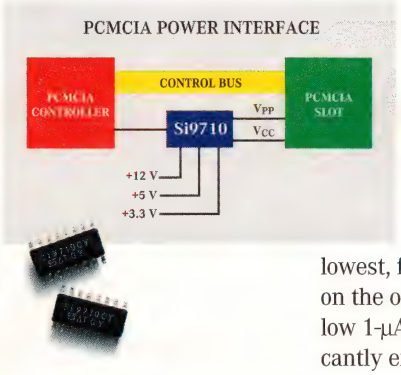

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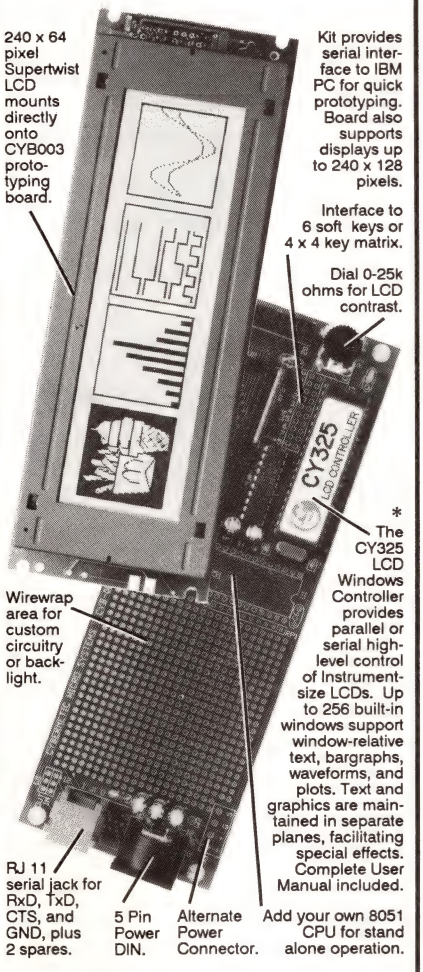
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READER SERVICE 166

THE RELIABILITY QUEST

In the last issue, I wrote glowingly about how the electronics industry has been a major contributor to the reliability of today's automobiles, and thus to a large degree responsible for the turnaround of the U.S. auto industry. The day after I wrote that editorial—the very next day—my five-year-old car conked out on the way to work, with the outside temperature hovering at 0°. The diagnosis: a failure in one of the electronic modules. The repair bill: $379. Welcome back to the real world.

The fact is that electronics has become an integral part of our everyday lives, from our telephones and television sets to the computers that dole out needed cash in the automatic teller machines. Over the years, these have become so reliable that most people take their operation for granted and are flabbergasted when they break down in the absence of a strong external force—a lightning strike, for example.

EEs, in particular, may place even more confidence in electronic systems than the general public. Barring component infant-mortality failures, most electronic systems operating in relatively benign environments should function for a long time, and they should at least outlive most of the system's mechanical parts.

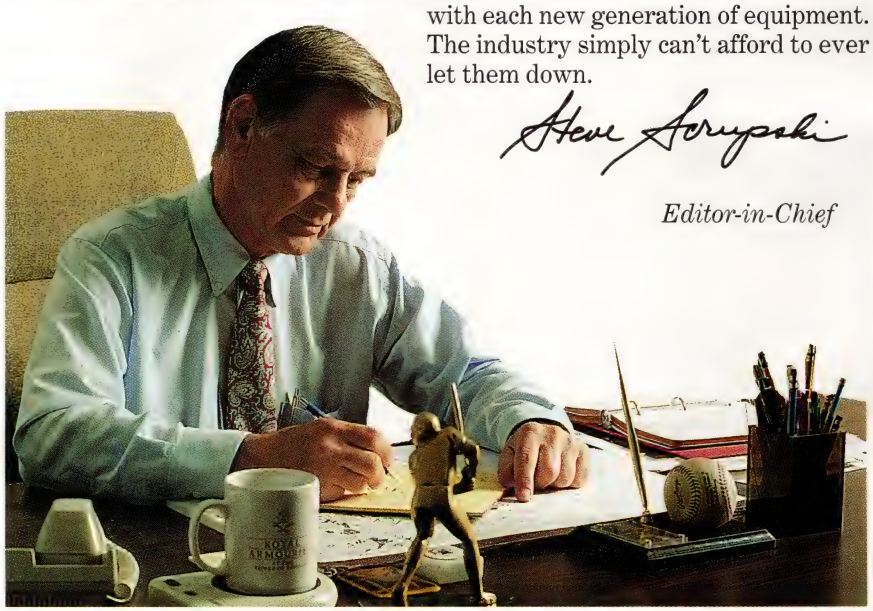
Clearly, the reliability of electronic systems is superior to that of most other technologies, and we have already demonstrated that electronic systems can be trusted to perform the most critical tasks. For instance, we're approaching the 25th anniversary of the Apollo moon landing, and, what's much more important, the subsequent landing back on earth. That feat couldn't have been achieved without its reliable life-support, guidance, and communications systems. It seems that most spacecraft failures were caused by other technologies, not electronics.

However, reliability, much like its counterpart quality, is something that can continually be improved, both from a design and a manufacturing viewpoint. My car has about 124,000 miles on it, and at an average speed over its lifetime of, say, 30 mph, that means that the electronic module operated reliably for about 4000 hours. This reliability probably is quite a bit improved over the first automotive electronic modules, but why shouldn't it last twice that long, or even longer?

Reliability is one of the major customer benefits offered by the electronics industry. More and more, the general public is becoming the primary customers for electronic equipment, and their expectations for reliable operation grow with each new generation of equipment. The industry simply can't afford to ever let them down.

Steve Serpiski

Editor-in-Chief



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1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	——	20	——	22	22	26
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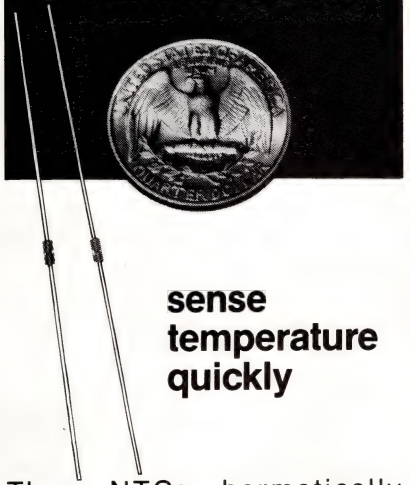

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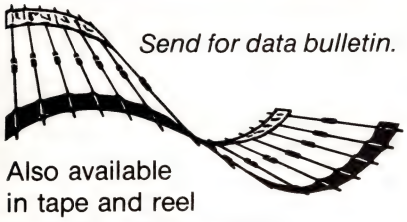

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READER SERVICE 90

GETTING IN TOUCH WITH USER INTERFACES

Once an afterthought to many designs, user interfaces to small computer-based devices—smart appliances, personal digital assistants, palmtop computers, and the like—are coming under closer scrutiny. To a large degree, consumer acceptance of the new devices hinges on an intuitive, efficient user interface. Input devices for these units must be light and ultra-thin to support a light, thin-profile device. But they also must be low cost, rugged, and able to operate in any position while consuming little power. Unfortunately, most input devices fall short in some key aspect.

However, a new breed of devices is beginning to hit the market that could revolutionize cursor movement. The technology is based on research into how humans instinctively use their fingers to point, press, and draw.

Devices such as mice, trackballs, and joysticks mimic these fluid motions by mechanical means. As a result, these devices generally are restricted to pointing, and drawing smooth lines with them can be a challenge. At full size, they're more suited for use on the desktop than on, say, the fold-down tray in an airplane seat. Miniaturizing them requires that their sensitivity be reduced to improve control. Tablets have been hampered by high cost and the need to use a keyboard for efficient data entry.

SHERRIE VAN TYLE
SOFTWARE

The new cursor technology, exemplified in a finger-touch surface developed by Cirque Corp., Salt Lake City, Utah, appears to hold promise in replicating human motions for cursor control. The device, called the GlidePoint, is based on work done by company president George Gerpheide at MIT in developing a dexterous robotic hand and in developing motion control and sensing systems at the University of Utah. The lightweight (12 g) GlidePoint pad is a thin (0.17 in.), rigid printed-circuit board laminate capped with a low-friction pointing touch surface on the top side and surface-mounted electronic components on the bottom surface. The pointing device requires no contact pressure—its field-distortion sensing works by measuring the capacitance of the human finger. In contrast, touch pads using membranes require consistent, high contact pressure and tend to wear out quickly and unevenly. On the GlidePoint's bottom surface are a custom ASIC, microprocessor, and analog components.

Gerpheide says that a cursor-pointing system can be thought of as consisting of four elements that make up a control system loop: the human controller, actuation, transduction, and controlled parameter. Each of these elements should be optimized for the most effective performance of a system.

The pointing and actuating operations, for example, shouldn't be too demanding on the user, limiting the amount of motion control to precisely place the cursor. A user should have convenient access (freeing up a mouse on a cluttered desk is inconvenient, of course), and left- and right-handed users should be equally comfortable using it. The device should require the fewest actions to perform an operation since each separate press is distracting.

In the transduction process, the device measures a user's action, translating it into the cursor's movement on the screen. Cirque's research shows that a typical mouse emits up to 8 counts per millimeter (200 counts/in.) of movement while human finger positioning seems to be about 20 counts per millimeter (500 counts/in.). Tracking speed determines the maximum actuation speed that can be transduced. A typical mouse can track hand motion up to 200 mm/s (8 in./s), while human finger movement achieves 1000 mm/s (40 in./s).

If GlidePoint, already licensed to several laptop PC makers, makes inroads at the expense of other devices, efforts will likely redouble to make other input devices more intuitive. Venture Development Corp. projects the sales of pointing devices, pens, touch screens, graphics tablets, and voice input to hit $815.7 million this year and $1.07 billion by 1997.

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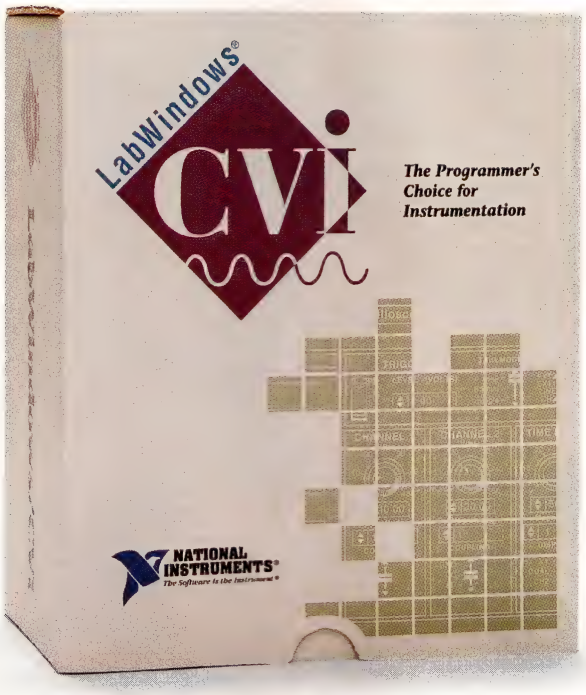

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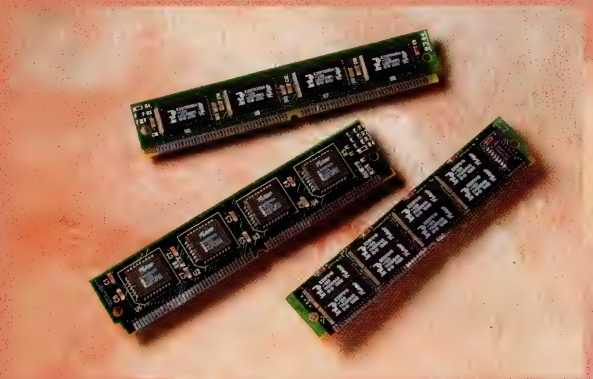

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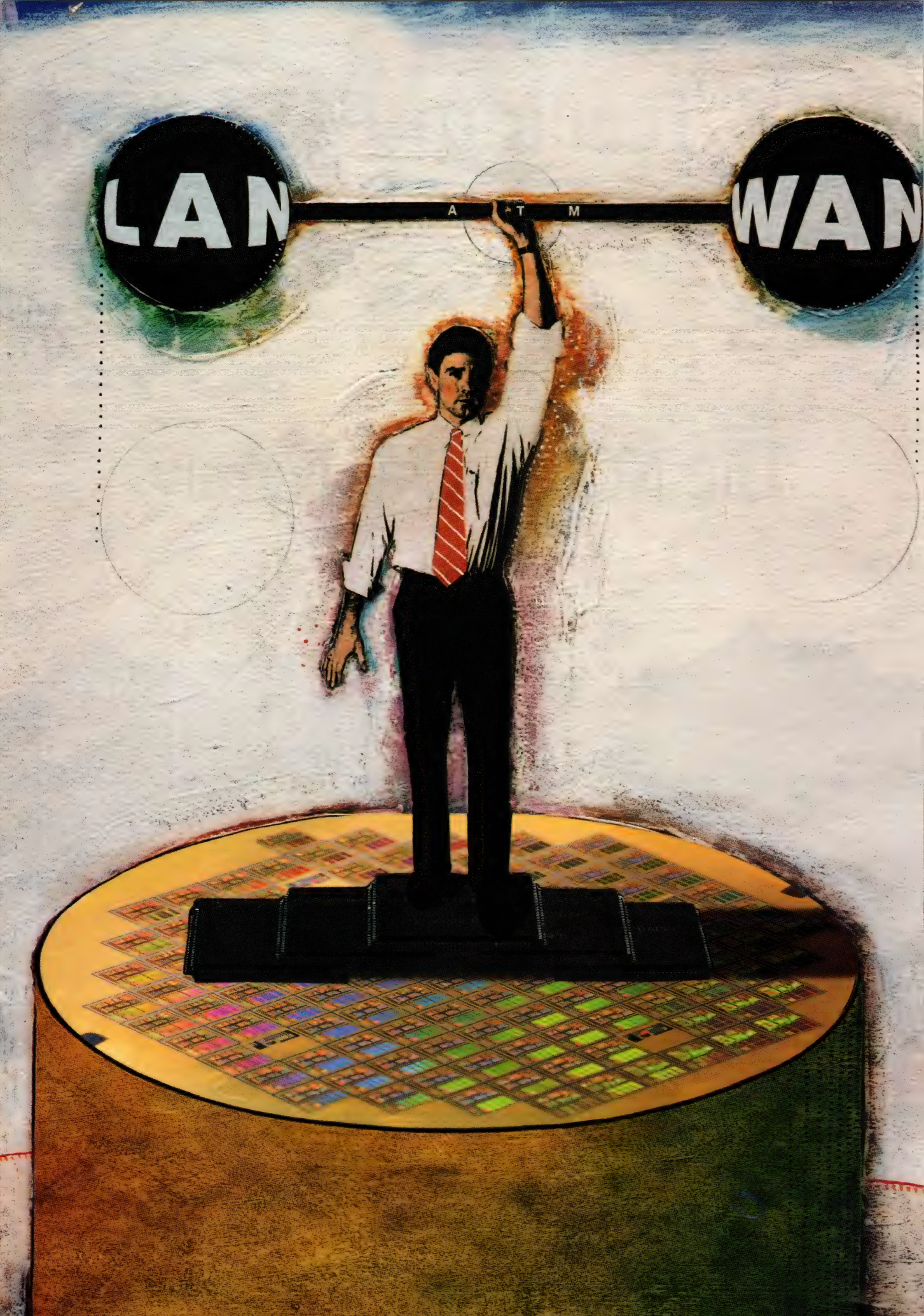
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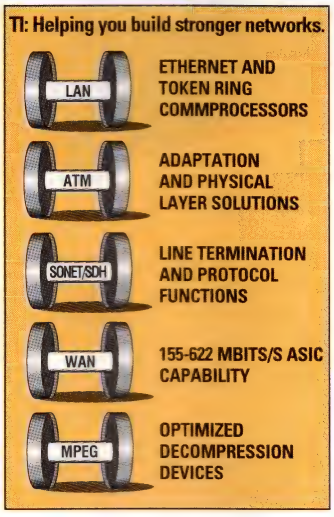

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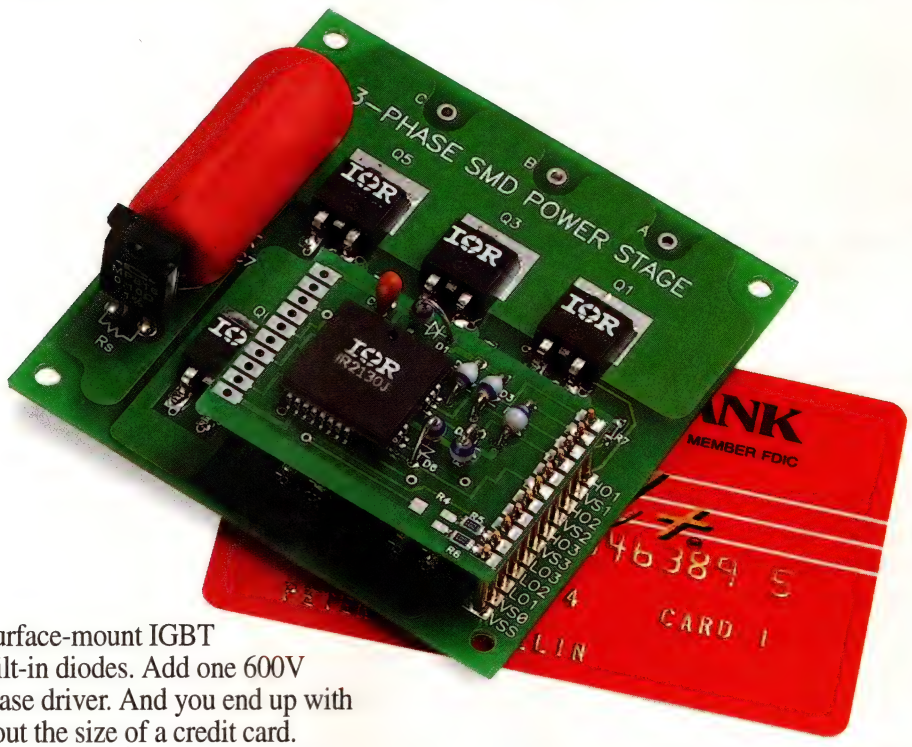

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TECHNOLOGY NEWSLETTER

SYNTHESIS LIBRARY YIELDS OPTIMIZED ICS

Thanks to a new library, users of Synopsys' synthesis tools can now automatically select cells that are optimized for the company's H4C submicron gate-array process without any manual intervention. The Motorola Component Library developed by Motorola's Semiconductor Products Sector, Chandler, Ariz., was created using Synopsys' DesignWare Developer. Components in the DesignWare Library include adders, comparators, multipliers, and over a dozen other cells. All of them are scalable for any bit width, and many components have two different implementations—one optimized for speed and one for area. In a comparison of a 255-bit carry-look-ahead adder synthesized with and without Motorola's DesignWare Library, DesignWare reduced the number of internal nets by 86%, cut the number of cells from over 2000 to 108, decreased execution time on a Sun Sparc2 computer by 32%, and improved the longest path delay from 102 to 17 ns. In addition, the reduced-cell count and smaller number of internal nets greatly simplifies physical layout, and should reduce the number of non-routable designs. For more information, call Motorola at (602) 814-4000, or Synopsys at (415) 962-5000. *LM*

GAAS MMIC TARGETS CELLULAR-PHONE DESIGNS

A 2-W, 900-MHz, radio-transmitter power amplifier could well be the first GaAs monolithic microwave IC (MMIC) destined for the mass-consumer market. The MMIC is part of the Sceptre five-chip set, developed by AT&T Microelectronics, Reading, Pa. The chip set, along with five filters, a microcontroller, an oscillator, and a low-noise amplifier, form a complete digital cellular telephone, which will be on the market by midyear. The set will be configured for telephones conforming with the European Groupe Speciale Mobile (GSM) standard, and later on with the 1.8-GHz, 250-mW, DCS-1800 standard. The set includes two 0.6-μm CMOS signal processors, a bipolar transceiver, a bipolar power-amplifier controller, and the MMIC. The chip set will be ready for sampling in the third quarter, with volume shipments scheduled for first quarter 1995. The target price is under $100 per set in million-lot quantities. Contact Charles Louisson, AT&T's European DSP marketing manager at +44 (0)344 865920. *PF*

90-mΩ PMOSFET FITS IN A 16-PIN TSSOP

By optimizing the lateral p-channel MOSFET in their LinBiCMOS process, designers at Texas Instruments, Dallas, packed a 90-mΩ p-channel FET—the TPS1101—in the 16-pin, ultra-thin, thin-shrink small outline package (TSSOP). TI typically uses the process for op amps and similar ICs. Unlike the more common n-channel vertical DMOSFETs, p-channel MOSFETs can be turned on and off with logic voltages. Their use in low on-resistance "power" switches (they can handle 1 A) eliminates the need for charge pumps to pull the FET's gate positive with respect to the source and the supply rail. Due to their low on-resistances, putting these FETs into skinny packages was quite a challenge. Multiple very-thin bond wires had to be employed along with multiple pins. For example, 5 of the 16 pins are connected to the FET's source terminal, and 5 to the drain terminal. It should be noted that the 90 mΩ is a typical value and requires –10 V between the gate and source for full enhancement. However, with the –4.5 V of gate drive provided by 5-V logic, and at a load of 1 A, on-resistance runs a maximum of just 170 mΩ. A drive of –2.7 V provides a maximum on-resistance of 320 mΩ while the FET passes 1 A. Although burdened with the lower mobility inherent in p-type devices, these FETs aren't slow. Switching 1 A into 10 Ω with 10 V of gate drive, they offer typical turn-on and turn-off delay times of 6.6 and 19 ns, and rise and fall times of 5.5 and 13 ns, respectively. Call 1-800-477-8924, ext. 4500. *FG*

LDO EMPLOYS P-CHANNEL MOSFET AS PASS DEVICE

Designers of linear power-control ICs are finally beginning to see the advantages gained by using p-type MOSFETs and bipolar devices. That's despite their lower mobility (reflected in lower speed and/or greater resistance for a given die size and voltage rating). Simply put, the p-channel FETs operate with minimum overhead and losses. And, p-type devices can be controlled with low positive voltages. For example, TelCom Semiconductor (formerly Teledyne Semiconductor), Mountain View, Calif., developed a family of CMOS low-drop-out linear regulators (LDOs) that uses an on-chip, lateral, p-channel FET as the pass device. The design combines a dropout voltage (the product of the FET's on-resistance and its load current) of 120 mV at 100 mA. Yet maximum quiescent current runs a mere 3 μA regardless of output current (250 mA maximum). Until now, design-

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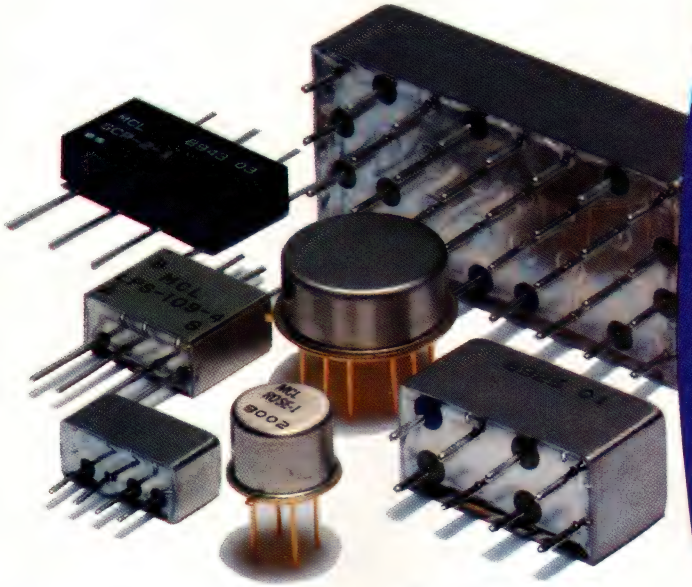

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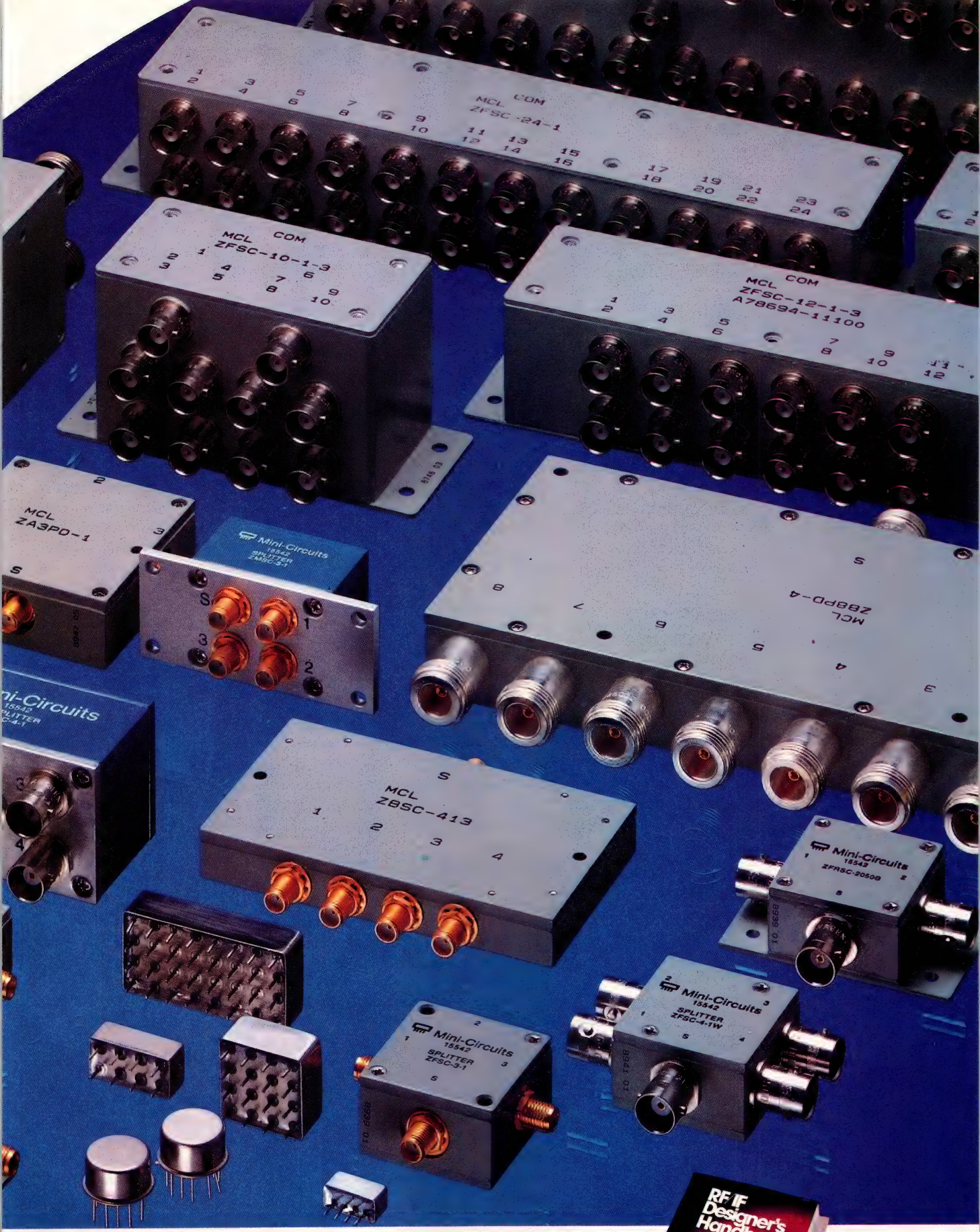

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F134 Rev D

ers of battery-powered systems looking for maximum efficiency have only been able to choose between LDOs built with npn or pnp output devices. The former offer greater efficiency as the drive current goes into the load, while the latter offer a lower dropout voltage, although their drive currents go to ground *(see "Tiny IC Plus FET Builds 'Super LDO' Regulator," p. 45).* Because the p-channel FET in the TC55 series of LDOs requires no drive current, careful linear CMOS design techniques achieve a low quiescent current. These LDOs, whose die size represents a trade-off between current rating, on-resistance, and package type, have been stuffed into tiny SOT-23s, SOT-89s, and TO-92s. Call Sandy McBride at (415) 968-9241. *FG*

Learn About High-Level Design And Simulation

High-level design and simulation are the subject of a series of educational seminars to be offered by Synopsys Inc., Mountain View, Calif., and its partners—NEC Electronics, Sun Microsystems, and Texas Instruments. The seminar is targeted at electronic system designers and engineering managers, offering attendees the latest design techniques. The topics include how to manage design complexity with high-level design techniques, how to shorten design cycles using one simulator from concept to sign-off, and how to incorporate design reuse to reduce risk and design time. Other subjects discuss simulation technologies and trade-offs, sign-off simulation, system-level modeling, debugging and analysis tools, and VHDL coding techniques. The seminar will be held in 12 cities across the U.S. throughout March and April. The tour starts in Irvine, Calif. on March 15. The cost of tuition for the full-day seminar is $95, and that includes all course materials, a copy of the *Simulation for High-Level Design* handbook, a copy of the book *Guide to VHDL*, a continental breakfast, and a lunch. Call (800) 388-9125 to register. Those who register up to two weeks before the seminar will receive a complimentary registration for a co-worker. *LM*

Ada Development Tools Target Fixed-Point DSP

Now that the first Ada software has been developed for a fixed-point digital-signal processor—Texas Instruments' SMJ320C50A—designers should reap the benefits of using a standardized and maintainable high-level language. In addition, they will be able to produce optimized code for real-time, large-scale complex applications requiring high processing capacity and low power consumption. That's the intent of an agreement between Tartan Inc., Monroeville, Pa., which develops high-level language compilers and tools for embedded, real-time applications, and Texas Instruments Military Products Div., Midland, Texas. Tartan previously developed cross-compilation tools for TI's floating-point DSP ICs: the 320C30, 'C31, and 'C40. The C50A cross-compilation system, including an optimizing compiler, a symbolic debugger (AdaScope), a librarian, and related tools hosted on Sparc workstations, is expected to be available in the fourth quarter. For more information, contact Tartan at (412) 856-3600; or TI at (915) 561-6500. *SVT*

Macro Generator Builds Efficient FPGA Blocks

A parametrized macro-function generator can produce structured blocks for FPGA designs that are much faster than those created by traditional synthesis approaches. Engineers will be able to use the ACTgen Macro Builder designed by Actel Corp., Sunnyvale, Calif., to construct efficient counters, adders, and other structured blocks. Developed as a productivity and performance tool for Actel FPGA users, the menu-driven software constructs macros that are tailored to users' designs in a fraction of the time needed for other approaches. And the macros are correct-by-construction, so users needn't write simulation vectors to verify the logic. The software targets the macros for each Actel device architecture while aiming to limit module count, maximize speed, and restrict loading to acceptable levels. ACTgen Macro Builder interfaces to popular CAE and high-level design tools and supports the emerging LPM standard. Call (408) 739-1010. *LM*

VHDL Standard Speeds Gate-Level Simulation

By strictly adhering to the Vital modeling standard, the Vulcan logic simulator innovated by GenRad Inc., Concord, Mass., can support the entire VHDL language while avoiding the slow gate-level performance that plagues many other VHDL simulators. Vital defines a set of VHDL primitives that are commonly used in ASIC cell libraries. It also defines a modeling style and a method for associating timing information with the cell primitives. Using a fully-compliant Vital simulator, it's possible to map the VHDL primitives directly to optimized internal data structures without fear of either violating the VHDL semantics or creating differences in results between various EDA tools. Once mapped to an internal representation, simulation can be accelerated using well-established techniques. In addition, simulation accuracy is delivered within VHDL through Vital's timing procedures and post-layout back-annotation mechanisms. Pricing for the Vulcan simulator, which runs on Unix workstations, starts at $20,000. Call (508) 369-4400. *LM*

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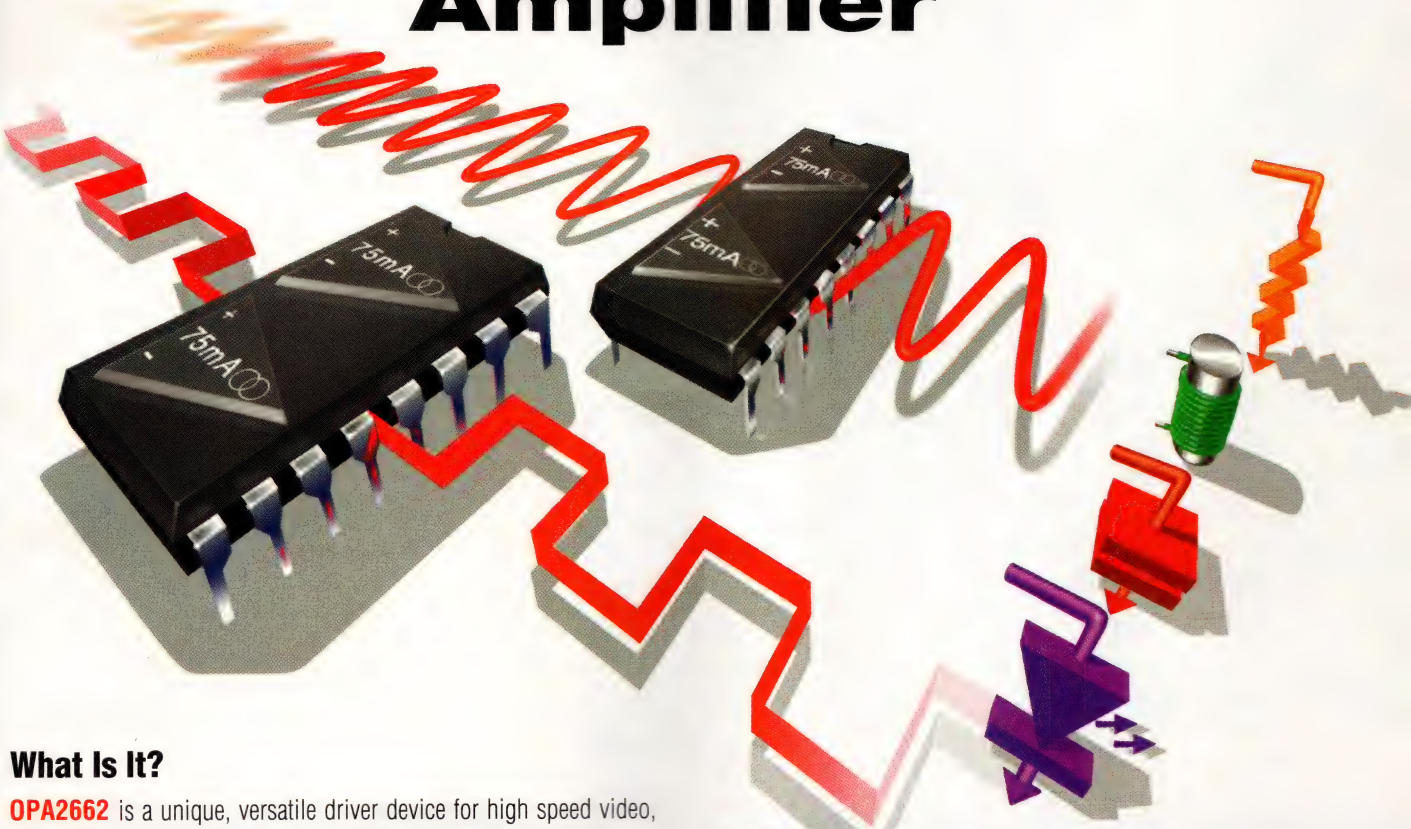


What Is It?

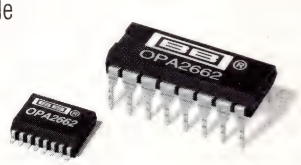
OPA2662 is a unique, versatile driver device for high speed video, broadcast, and communications applications where a load current, rather than a voltage, must be controlled. It combines two voltage-controlled current sources—each can convert an input voltage into output current with up to ±75mA drive capability—or double it by connecting the outputs in parallel. **OPA2662**'s flexibility, power, and low cost make it the driver amp of the future.

Where's It Used?

Use **OPA2662** as a driver amplifier for many kinds of loads—resistive or complex—in applications like magnetic recording heads, RF power output stages, and digital transmission systems. Or, use the enable mode to create a switchable 75Ω/50Ω line driver, or a 2-to-1 or a 1-to-2 multiplexer, or a bi-directional configuration for RF distribution systems. **OPA2662** helps simplify complex signal processing designs—its superior for video systems, a variety of high speed optical applications such as driving LEDs or laser diodes, and data acquisition circuits. Let the power of **OPA2662** drive your next application.

OPA2662 Key Specifications

- Bandwidth 370MHz
- Digital transmission rate. 400Mbits/s
- Slew rate (current) 58mA/ns
- Output drive (per channel) ..... ±75mA
- TTL-Enable (on/off-time) 30/200ns
- Packages ..... 16 pin-DIP and SOIC
- Evaluation board available



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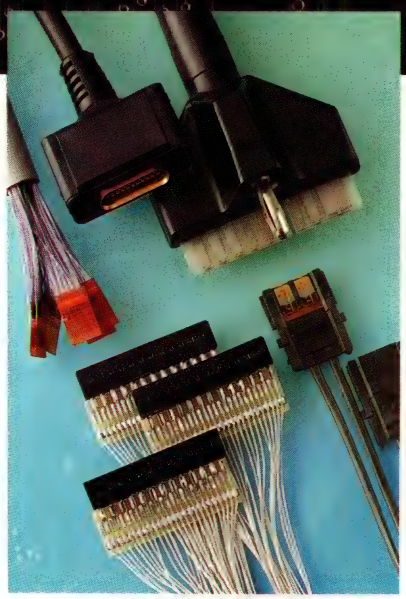

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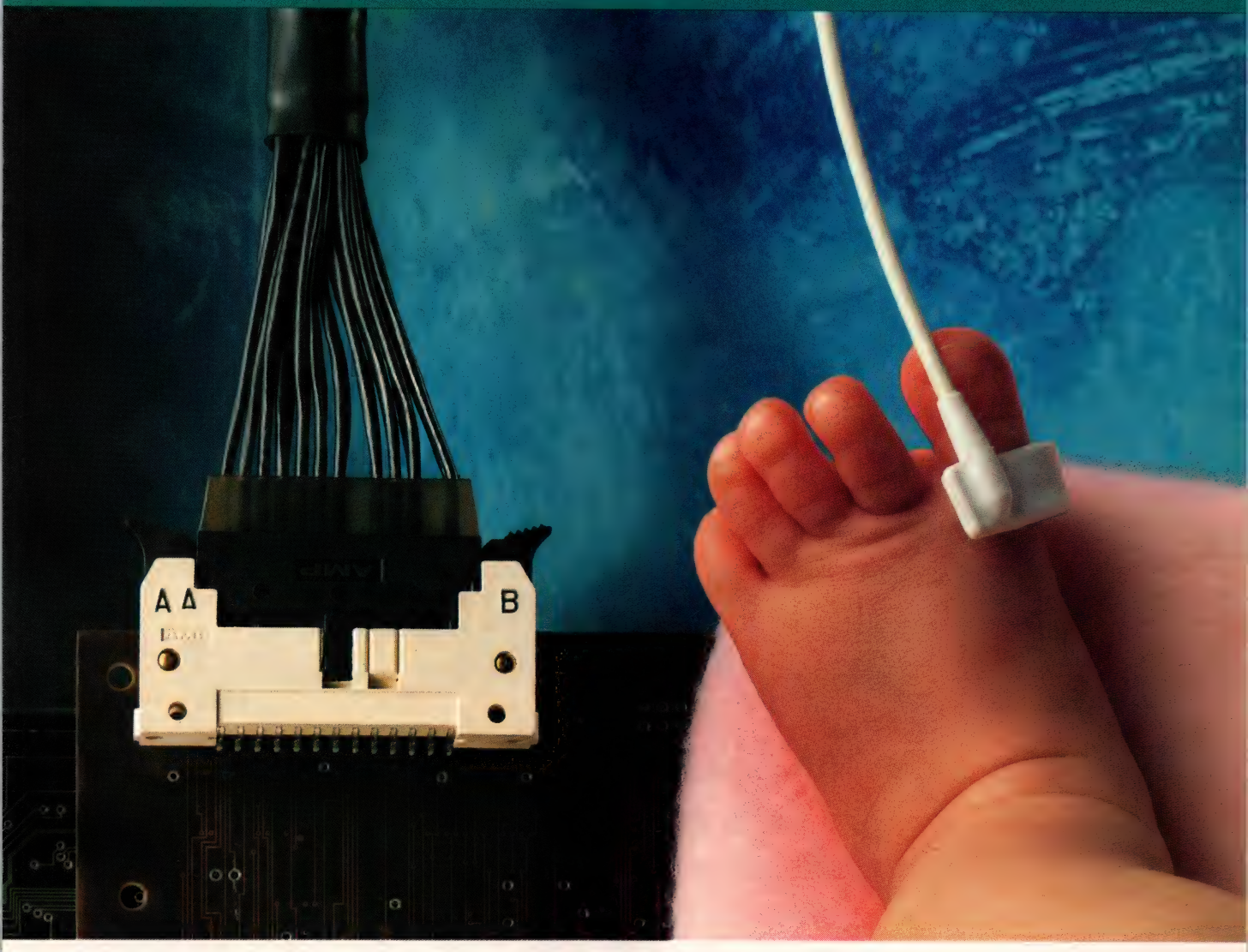

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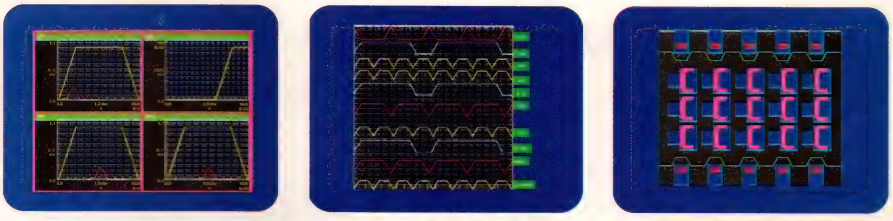

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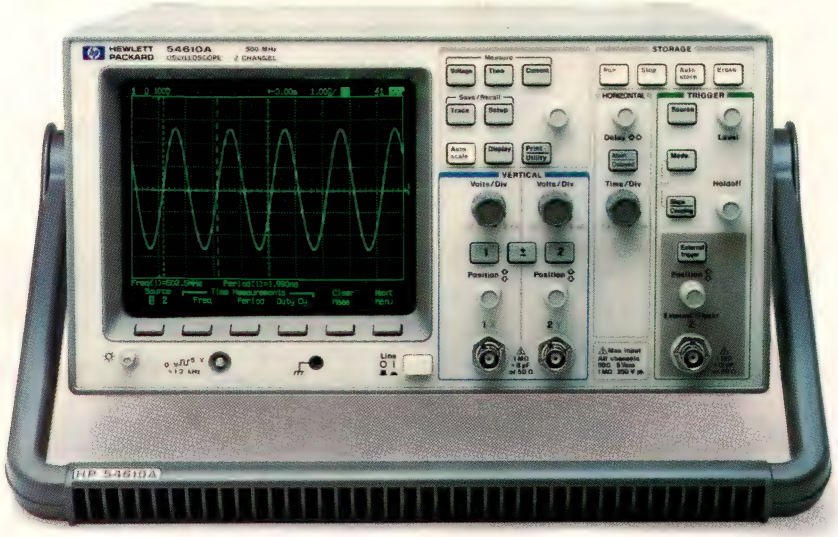

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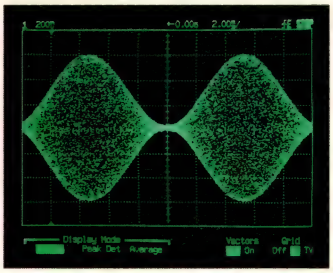

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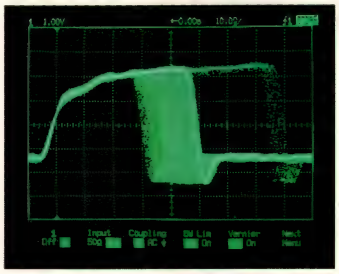

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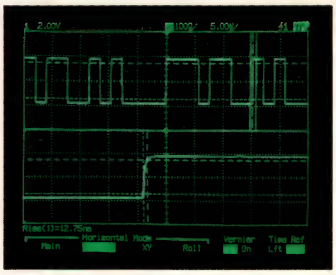

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PIEZOELECTRIC BIMORPHS AND FIBER OPTICS FUEL LARGE-AREA OUTDOOR DISPLAYS

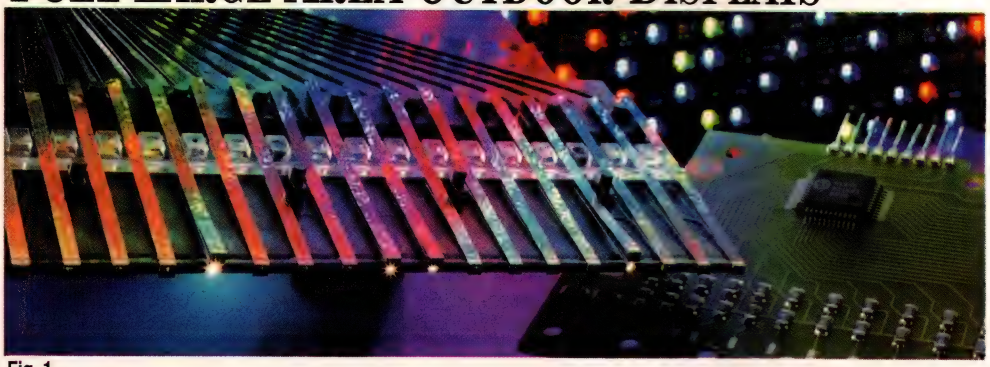


Fig. 1

A new approach to large-scale outdoor electronic displays, such as stadium scoreboards and information displays in transportation centers, capitalizes on a marriage of piezoelectric technology and fiber optics. The display technology is based on light shutters composed of strips of piezoelectric film that cover or uncover the ends of optical fibers in response to precisely-timed voltages. Ultimately, it will generate high brightness and resolution levels that have been difficult to achieve in large-scale displays up to now.

The fiber-optic display technology, developed by Sunfire Europe S.A., Brussels, Belgium, is intended as an alternative to existing technologies for outdoor displays like LEDs, light bulbs, phosphor-based displays, liquid crystals, and video walls. It overcomes many of the pitfalls of existing approaches while retaining or even improving on some of their strong points.

At the heart of the display lies a 175-by-175-mm module that consists of 30 shelves. Each shelf contains 30 optical fibers spaced 5.7 mm apart. In back of the module, the fibers are collected in three bundles using a funnel.

The bundles are illuminated by a metal-halide, small-discharge lamp through an optical device. That lamp itself represents a new technology developed by General Electric at its Lena Park facility, Cleveland, Ohio, in cooperation with Sunfire. According to Sunfire, the lamp is the brighest available. The optics split the lamp's light into its red, green, and blue components and provide for uniform illumination of the fiber bundles *(Fig. 1)*.

After the fibers bring the light from the back of the module to the front panel, the piezoelectric light shutters take over. The shutters, or light gates, are made up of two strips of 27-µm piezoelectric film glued together with a 10-µm adhesive layer. In this configuration, the strips form a bimorph, or bimetallic strip. The gates measure 2 mm wide by 2 cm long.

With an application of 250 V dc, the upper piezoelectric-film layer shrinks and the bottom layer expands. The net result is a curling effect that raises the shutter by 2 mm. Depending on the voltage's polarity, the shutter will either rise or fall in front of the fiber tip, and thus cover or uncover the light source *(Fig. 2)*.

Rise and fall time of the shutters is less than 3 ms, more than fast enough to switch the light output on or off during a video-frame interval. According to Sunfire, only liquid-crystal shutters can compete with this on-off time. But they suffer from high cost and difficult production.

A full-size screen is assembled from up to 36 modules, with which a screen can be juxtaposed to any size and form. The front face is uniform and there's no visible junction between modules.

By making trade-offs in color resolution for spatial resolution, three pixel types are possible—a video pixel and two graphics pixels. The video pixel, measuring 17 mm across, is the preferred pixel for video screens measuring a minimum of 12 meters square.

Of the two types of graphics pixels, one provides 16 colors with a pitch of 11.4 mm, and is well suited for computer-graphics animation. The other offers eight colors but has the highest resolution of all three, and is useful for logo animation.

The real-time front-end electronics can be located remotely in video applications. In graphics applications, the screen can be linked to computers by Ethernet, a serial link, or switched or by Integrated Services Digital Network (ISDN) telephone lines.

In the video mode, gray scales are generated by combinations of space modulation, time modulation, and a real-time halftoning algorithm. Because of its fully digital nature, the screens can mix video and computer graphics.

In building its bimorphs, Sunfire took advantage of advances in piezoelectric-film technology at AMP Sensors, Valley Forge, Pa. The film is producible in very high volumes and at very low cost. Also, it's important that the bimorphs be very flat and withstand high temperatures.

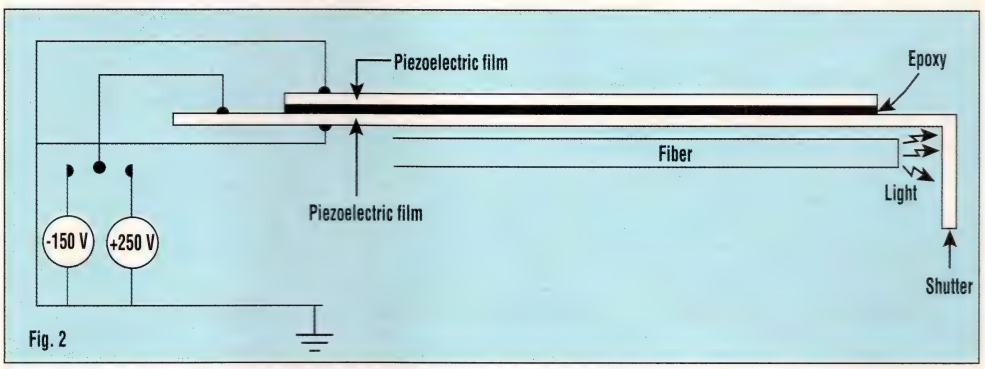


Fig. 2

AMP Sensors developed a production approach that anneals the film at higher temperatures than in the past and uses an ultra-uniform stretching process to produce uniform film. Otherwise, each element would have to be individually calibrated and controlled.

For more information about the display system, contact Jean Pierre Vanderregdt at Sunfire Europe S.A., at 32-2-215 58 20. For more information about the piezoelectric film, contact AMP Sensors at (215) 666-3500.

DAVID MALINIAK

MOSFET-DRIVER'S DESIGN CUTS "SHOOT-THRU" LOSSES DURING OUTPUT-STAGE SWITCHING

Power MOSFETs have become virtually ubiquitous, particularly for the control of moderate power levels. They're usually driven by 5-V (and even 3-V) logic signals. As a result, multiple families of a new kind of MOSFET driver ICs have become available. The drivers level-shift the low-voltage logic signals to the 10 V or more needed to fully enhance the n-channel power FETs (so they can achieve the lowest on-resistance) and provide the power to charge and discharge FET gate capacitances at high speed.

However, in many applications such as switching regulators and drivers for p-i-n diodes and CCDs, as MOSFET switching speeds climb above 1 MHz, serious problems are arising. Driver-IC power dissipation is increasing due to switching losses (driving gate capacitances and "shoot thru" losses); logic signal sources are being loaded down as ac input impedances drop; logic thresholds are becoming less well defined; and noise immunity is falling. To combat these problems, Bruce Rosenthal of Elantec, Milpitas Calif., came up with a new architectrue for CMOS high-speed MOSFET drivers *(Fig 1)*.

To put the switching problem into perspective, consider that until recently, most designers equated CMOS ICs with low power. But as continuous switching speeds have risen, losses caused by the need to charge the parasitic capacitances on all toggling internal nodes has belied the earlier "conventional wisdom". Much to the sorrow of many designers using the latest high-speed processors, the following equation still holds:

$$P = CV^2f$$

where P = power loss; C = node capacitance; V = supply voltage; and f = the switching frequency.

This equation governs CMOS circuit power dissipation. Additionally, so-called "shoot-thru" losses occur in CMOS inverters during the portion of each transition (from low to high or high to low) when both the p-channel and the n-channel FETs conduct.

Several factors compound these switching losses in high-speed MOSFET drivers. For starters, to charge and discharge the gate capacitance of the FETs at high speed, MOSFET driver output impedance must be low, on the order of a few ohms. In addition, rather than switching logic levels, the output stage of a FET driver switches 10 to 15 V. Thus "shoot-thru" losses become significant, as defined by :

$$P = 2fV \int_0^t I_{(t)}\,dt,$$

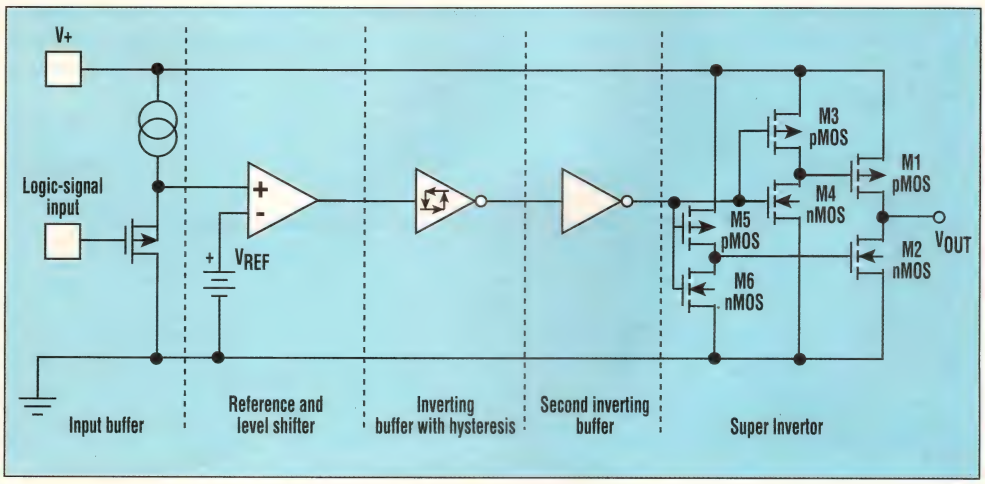
where I_s = "shoot-thru" current; and t = duration of "shoot-thru".

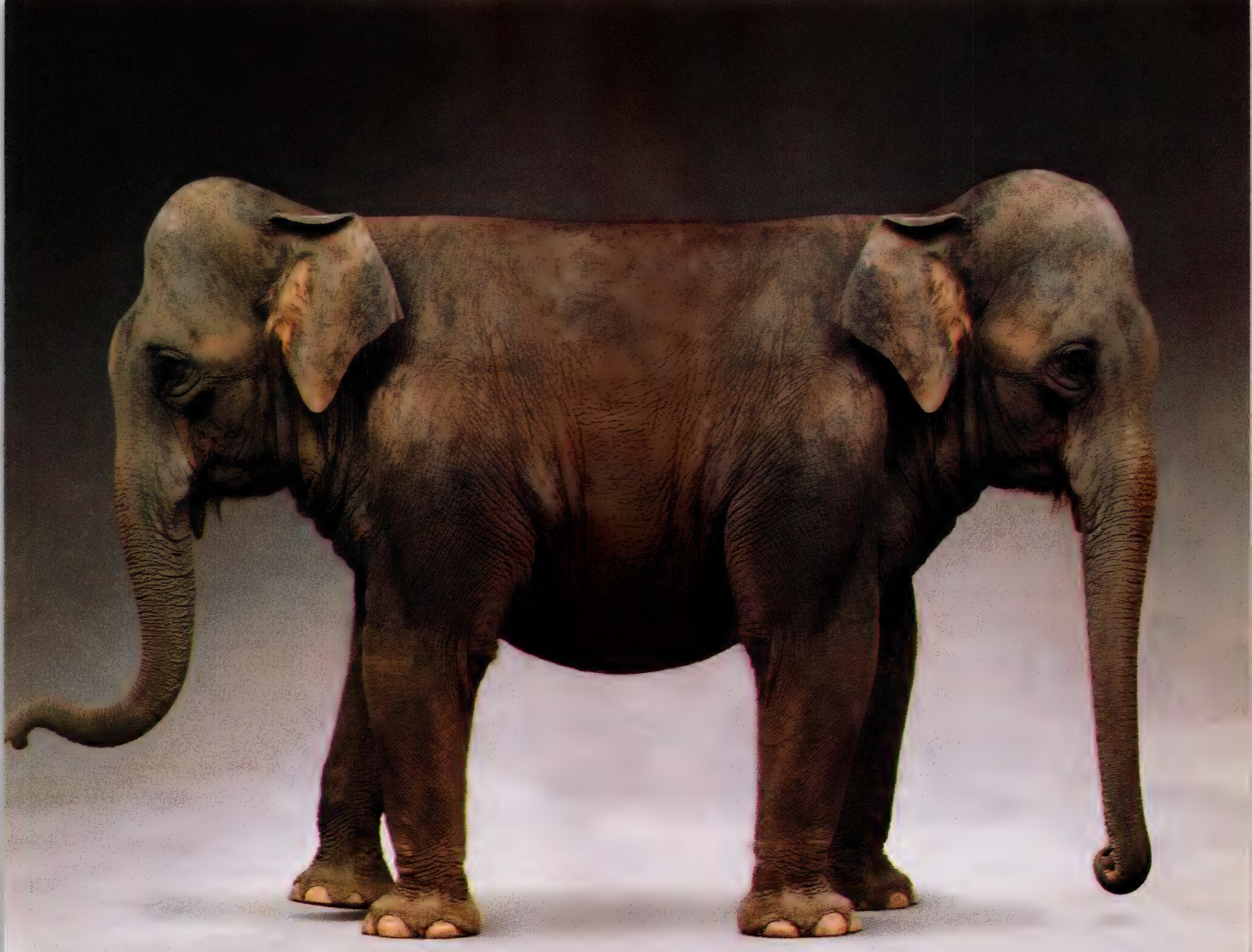
To minimize "shoot thru" losses, Rosenthal came up with the "Super Invertor". This 6-FET (rather than just two FETs) output stage employs brake-before-make switching to beat "shoot thru". He delibrately unbalances the FETs driving transistors M3-M6, which in turn drive the output devices M1 and M2. Specifically, M4 is weaker than M3 to ensure that M1 turns on slowly during a normal turn off. Similarly, M5 is weaker than M6, to slow the turn-on of M2.

"Shoot thru" losses can be traded off against propagation delay. In addition, the output impedances to both supply rails are matched (8 Ω maximum), to ensure equal rise and fall times.

To operate with inputs from moderately high source impedances, the drivers must provide high dc *and* ac input impedances. Putting a p-channel source follower on the front end of the new driver keeps its input impedance high. The follower's inherent "bootstrap" effect eliminates both the FET's gate-to-source capacitance and the Miller capacitance at the gate. Only the gate-drain capacitance of the p-channel input FET remains to load the signal source. The follower's current-source load is set by a dc reference voltage.

The MOSFET-driver's input stage is followed by a reference-based logic-level sense circuit and level shifter which detects input signals and translates them to a rail-to-rail swing of 10 to 15 V. Ths is followed by an inverting buffer with hysteresis which raises noise immunity. This buffer drives a second inverting buffer which provides the output current required to rapidly charge the





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gate capacitance of the four FETs (M3-M6) at the input to the "super invertor".

Specifications for the resulting drivers (Elantec's EL7200 series) are impressive *(Fig. 2)*. Clocked at up to 10 MHz and running off 15 V, they can put out the 2-A peak pulses required to charge or discharge 1000 pF to over 10 V in under 20 ns. Turn-on and turn-off delay run a maximum of 20 ns. The output can handle 100 mA continuously yet quiescent current is just 2.5 mA maximum. The output also tristate capability.

The drivers are built on an 18-V silicon-gate process and can operate from 4.5 to 16 V. To achieve high current densities, the large output devices on the die employ a two-dimensional (lateral) polysilicon-gate structure which resembles a waffle. The design has made possible cramming a pair of drivers into SOICs and 8-pin DIPs. For additional information about these MOSFET drivers call (408) 945-1323.

FRANK GOODENOUGH

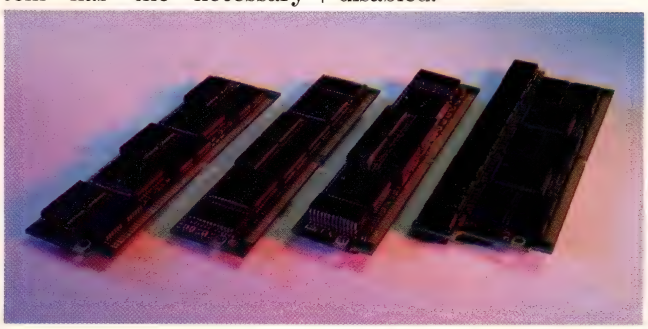
MEMORY-EXPANSION SIMMS ADD ERROR CORRECTION

PCs that employ single in-line memory modules (SIMMs) for system memory expansion now can take advantage of automatic error-correction code (ECC). IBM's Microelectronics Division, located in Hopewell Junction, N.Y., has come up with SIMMs that employ ECC within the modules themselves. The company claims that users need only replace their existing SIMMs with the IBM-developed SIMM devices to gain the ECC capability.

ECC is presently built into many computer systems. These are typically high-end servers, where the ECC resides in the memory controller as part of the chip set, and the SIMMs contain a few extra bits to support the ECC capability. A JEDEC standard for ECC-optimized SIMMs exists for this type of architecture, but it requires the extra baggage of placing some of the intelligence in the memory controller. Thus, unless the system has the necessary built-in logic to support the ECC capability, using conventional SIMMs for memory expansion can't give that support.

The SIMMs developed by IBM are fully retrofittable for upgrading existing systems and are built to standard timing specifications. They conform to the architecture and pinout of the JEDEC standard for "by-36" 72-pin parity SIMMs. Four different organizations are offered over the range of 1 Mbits by 36 bits (4 Mbytes) through 8 Mbits by 36 bits (32 Mbytes). Each is available with either 70- or 80-ns timing. In addition, IBM's SIMMs can be combined with parity SIMMs because the two are pin-compatible and functionally identical. The parity is checked on incoming write operations to ensure that corrupt data isn't being received.

Non-parity applications also are supported, such as those used in Macintosh computers. In this case, the parity-checking feature is disabled.



Typically, SIMMs contain eight DRAM chips and a parity-bit DRAM. The ECC of a SIMM device has 12 DRAMs for data and 4 ASICs to handle the ECC and some of the control functions, making an ECC-capable SIMM somewhat more expensive than a standard SIMM.

IBM's SIMMs will correct any occurring single-bit errors. They also take care of hard errors due to defects in the silicon, as well as soft errors caused by high-energy cosmic rays or alpha particles that could originate in the DRAM packaging material.

The SIMMs can correct on a byte boundary, which means that if a processor tries to write just one byte of data (such as to transfer data from the floppy disk drive), the SIMM doesn't have to implement a read-modify-write function. Instead, it simply writes that byte of data. Because a custom ECC algorithm is implemented on an ASIC and high-speed DRAMs are employed, no performance hit is encountered.

Basically, any computer platform that isn't built with native ECC, yet ends up handling a critical operation, can employ IBM's SIMMs. Because the latest generation of operating systems are more taxing on memory than previous software, some memory defects tend to show up that might not be noticeable in a system that just runs DOS. For a typical 16-Mbyte system, SIMMs with ECC offer a 60-times improvement over standard SIMMs.

In the PC environment, each data byte has four associated check bits. The code scheme employed by the ECC on a SIMM requires 60% more memory—hence the extra DRAMs. This permits single-error correction on each data byte, and results in four separate ECC words on each SIMM.

But the extra DRAM chips results in a slightly larger package than that used for standard SIMMs. JEDEC-standard SIMMs measure 4.25 by 1 (or 1.2) by 0.36 in. For those cases where the system maker can't accept a taller module, IBM employed its stacked, small-outline J-leaded (SOJ) package DRAM technology. It doubles the card's density and adds thickness, but doesn't increase the area. Because package pitch in 16-Mbit-based SIMMs is important, a package height of 1.7 in. is used. *(see the figure)*. The modules are manufactured with either gold or tin tabs.

Though initially developed for IBM systems, the IBM SIMMs will now be made available to the industry, primarily focusing on OEMs. Samples are available now, with production to begin shortly. Prices range from $276 for 4 Mbytes to $2671 for 32 Mbytes.

For more information, call IBM Microelectronics at (800) IBM-0181, ext. 904.

RICHARD NASS

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SUBSTRATES PUSH LED LUMINOUS EFFICIENCIES BEYOND THOSE OF INCANDESCENT LAMPS

A transparent substrate has made it possible to produce LEDs that surpass incandescent lamps in energy efficiency, reliability and cost. In fact, they're twice as bright as available high-performance LEDs. Transparent-substrate aluminum-indium-gallium-phosphide (TS AlInGaP) technology hinges on the ability of the gallium-phosphide (GaP) substrate to allow significantly more light to be emitted from the diode rather than be absorbed by the substrate material.

Currently available high-performance LEDs consist of an active AlInGaP layer sandwiched between an upper GaP window and a lower GaAs substrate. This type of device, referred to as absorbing-substrate (AS) AlInGaP, effectively increases the efficiency of amber-colored LEDs.

Unfortunately, problems with internal absorption of light have made it virtually impossible to produce higher efficiency AS LEDs. On average, for every 20 electrons that go into the chip, 1 photon of light is extracted out and emitted. This results in semiconductor chips with low extraction ratios or R_es (R_e = light efficiency into the device per light efficiency out). However, no existing AS device can produce an R_e of much more than about 0.1, the maximum that can be achieved. Consequently, AS LEDs haven't been able to compete with incandescent lamps.

The Components Group of Hewlett-Packard Co., San Jose, Calif., decided to take a fresh approach to this dilemma and developed a new TS AlInGaP technology. This method focuses on increasing the R_e of a LED by allowing incoming light to pass through the chip, as opposed to being absorbed by it. This allows for a two-fold improvement over current LED technology. By fine-tuning the LED structure, an estimated additional 20% improvement is forecast over the next few years. As a result, small lightweight LEDs in a variety of very bright colors can be fabricated for a number of different applications.

The primary advantage of TS AlInGaP technology is that for the first time, it allows LEDs to outperform incandescent lamps in low-power applications. Not only do LEDs have higher luminous efficiencies, they also consume less power and are dramatically more reliable *(see the figure)*. While the typical incandescent lamp burns out after 1 to 10,000 hours of operation, the TS AlInGaP LED lasts over 10 million hours. Subsequently, the overall cost of supplying power to these LEDs, as well as taking care of all maintenance, is quite low when compared with incandescent lamps.

The key to manufacturing TS AlInGaP LEDs is the ability to produce a transparent GaP substrate. Another key factor is being able to substitute the GaP substrates for the light-absorbing GaAs substrates used on AlInGaP LEDs.

TS AlInGaP production involves several basic steps. First, crystal GaP ingots are grown. Each ingot is sliced into 15- to 20-mil-thick wafers, which are then polished and prepared for use as substrates for an epitaxial-film process.

The AlInGaP epitaxial film is grown by metal-organic vapor-phase epitaxy (MOVPE), where a gaseous form of the material to be grown (AlInGaP) is transported via a metal-organic gas, such as trimethylgallium (TMG). Then it's deposited onto a substrate wafer located in the hottest part of a growth chamber and surrounded by relatively cool walls. Next, the transparent GaP substrate with its epitaxial layer goes through a series of final wafer fabrication and assembly processes, with the end result being a wafer filled with TS AlInGap LEDs.

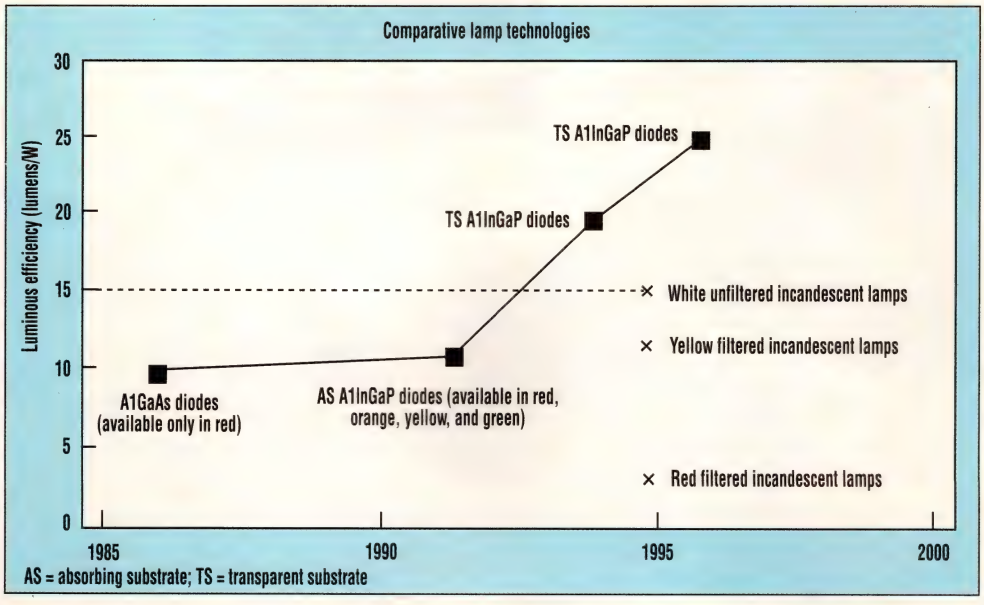
The only downside to TS AlInGaP technology is that it can't produce LEDs for high-power requirements. A typical LED operates with an input power of about 0.1 W. In comparison, a typical light bulb has an input power of approximately 60 W. Consequently, it takes a large number of LEDs to produce the same amount of light you could receive from just one light bulb.

However, there are still many applications where power-hungry incandescent lamps aren't always the answer. And, as the technology continues to change and improve, it's not inconceivable to imagine LEDs one day replacing incandescent lamps in everyday applications.

First production units pf the TS AlInGaP LEDs will be available around June.

For more information, contact Hewlett-Packard Co. Inquiries, 5301 Stevens Creek Blvd., P.O. Box 58059, Santa Clara, CA 95052-8059; 1-800-537-7715, ext. 8003.

CHERYL AJLUNI



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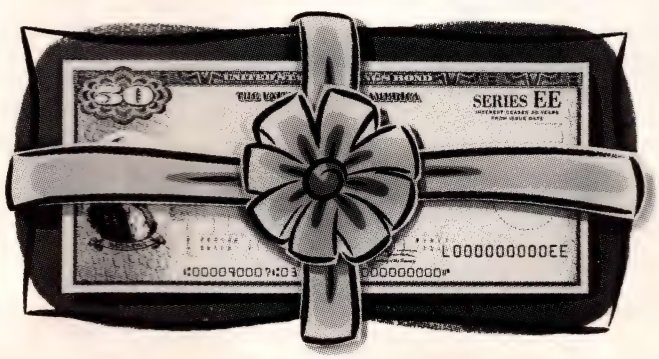

In The World Of Hybrid Microelectronics, Bigger Is Better.

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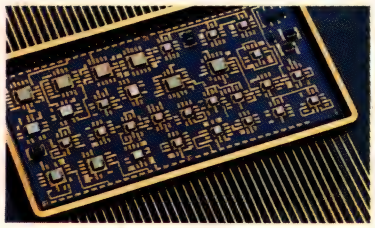

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TINY IC PLUS FET BUILDS "SUPER LDO" REGULATOR

LOWEST-DROPOUT LINEAR-REGULATOR ICS CONTROL CURRENTS FROM MILLIAMPS TO TENS OF AMPS WITH AN ON-CHIP SUPER-β PNP DEVICE OR A POWER FET.

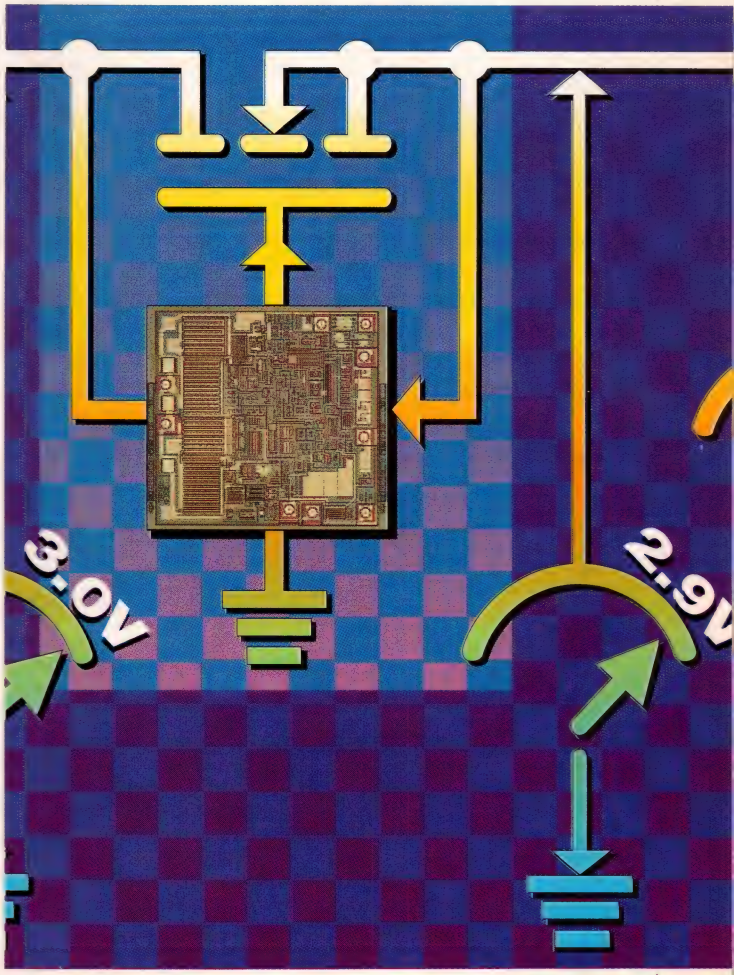
FRANK GOODENOUGH

The low-dropout regulator (LDO) has evolved from the humble three-terminal linear regulator ICs designed by Widlar and Dobkin over 20 years ago to today's device with its superior performance. While the dropout voltage of a typical linear regulator runs between 2 and 3 V at rated current, a typical LDO drops out somewhere between 800 and 1500 mV, depending on whether it uses a pnp or an npn as a pass transistor. However, the maximum rated current of available LDOs stops at about 1.5 A.

Such performance may be impressive enough for some applications, but it doesn't fulfill the needs for many others. There's an outcry for even lower LDO dropout voltages and higher rated currents. To satiate those needs, Micrel Semiconductor came up with a pair of technologies that both lower LDO dropout voltages and increase their current rating by at least an order of magnitude.

One technology employs Micrel's advance in process technology, the "Super beta pnp." The other implements one of those "Why didn't I think of it?" ideas with a unique IC, the MIC5157. Just combining the correct n-channel power MOSFET with the MIC5157 creates an LDO that handles any desired current while providing dropout voltages as low as needed, even just a few millivolts *(Fig. 1)*. Between them, these new LDOs provide system designers with full-scale ranges of LDO performance. Micrel dubbed the MIC5157 the "Super LDO" regulator *(for additional information, see "All about LDOs," p. 48)*.

Several major forces are spurring on the move to LDOs, particularly to those with lower dropout voltages and higher currents:



- Efficiency is the watchword of today's system designers, whether they're working on portable/battery-powered products, "green" systems, or even the ever-smaller ac-line-powered instruments and systems.
- Power dissipation and the heat associated with it must be limited in all such systems for many reasons, including the elimination of bulky heat sinks. Power dissipation of 3 W (3

V at 1 A) is not acceptable. And 30 W (3 V at 10 A) is out of the question.

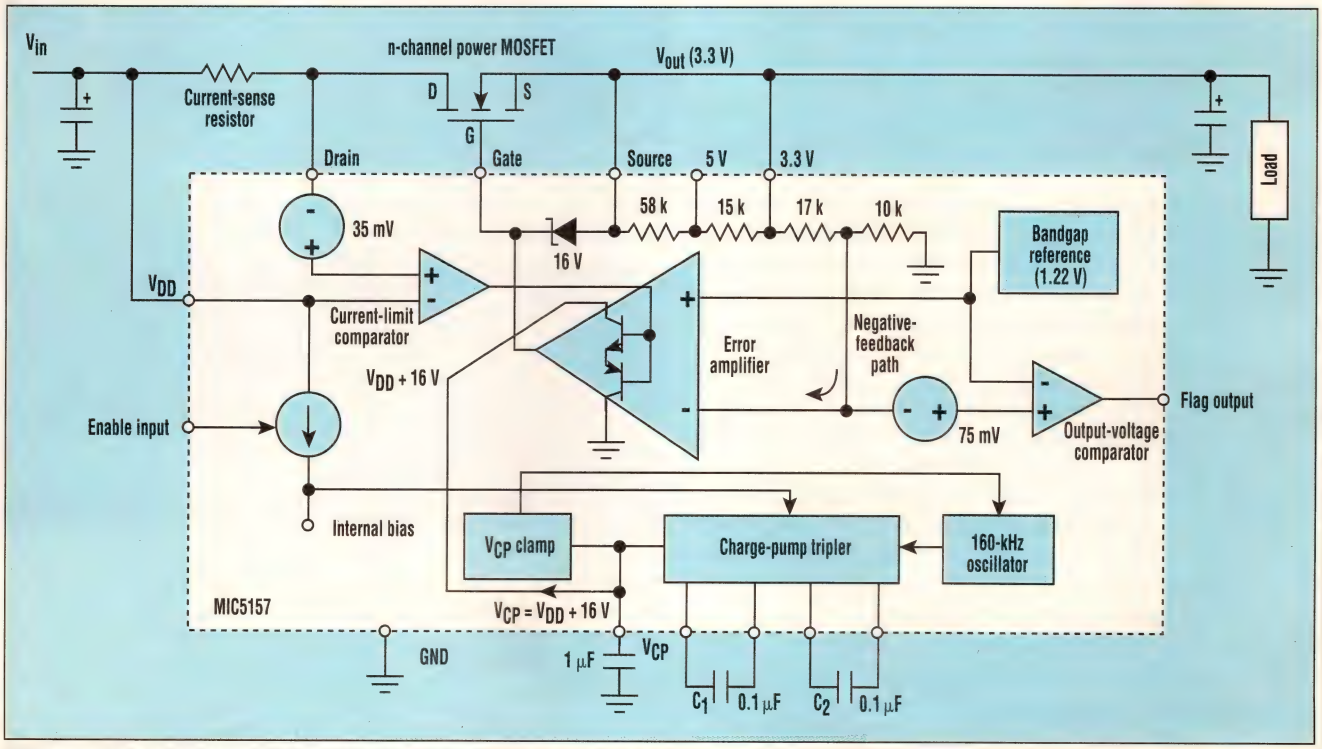
- The move to ever-lower supply rails with no end in sight, at increasingly higher currents, necessitates mixed-supply-voltage systems. The LDO represents a cost-effective way to convert a higher-voltage supply rail to a well-regulated lower voltage. For example, a linear regulator converting a 5-V ±10% rail to a 3-V ±5% rail—regardless of current—can't reliably employ a regulator with a 1.5-V dropout.
- In many of these applications (like battery-powered systems), the input voltage can drop significantly over time or for short periods of time. The input voltage for battery-powered systems like those in vehicles also drops significantly when exposed to low temperatures—e.g., the "cold-crank" condition. As the input voltage drops, the LDO must maintain regulation with minimum "headroom" (input-to-output voltage).
- LDOs with Enable inputs act as regulating-switches to perform power-management functions in systems from notebook PCs to vehicles.

Essentially, the MIC5157 employs the MOSFET as the pass transistor in a conventional negative-feedback regulation loop. In addition, it inserts a critical fixed boost (offset) voltage within the control loop. The boost voltage, created by a voltage-tripling charge pump, keeps the FET's gate well positive with respect to its source, regardless of the FET's drain voltage (V_{in}). The charge pump implements the boost voltage by providing a high-voltage supply rail (V_{CP}) for the error amplifier's output stage. It in turn drives the gate of the power FET. V_{CP} is clamped to V_{in} + 16 V. Keeping the n-channel MOSFET's gate well positive with respect to its source keeps its on-resistance at a minimum as the input voltage drops and/or the load current rises.

At any output current, the minimum dropout voltage of an LDO regulator built with the MIC5157 is the product of the FET's minimum on-resistance, $R_{DS(on)}$, and the FET's output current. For example, when using a FET with a 10-mΩ on-resistance, the dropout voltage for a current of 20 A will be just 200 mV. As current increases, dropout voltage follows it *(Fig. 2)*. FETs are available with on-resistances even lower than 10 mΩ, and they can be paralleled.

Due to their ability to regulate virtually unlimited current, these Super LDOs will be involved in quickly upgrading existing 5-V systems, allowing them to use current-hungry, lower-voltage versions of today's advanced processors. These include DEC's Alpha, IBM's Blue Lightning, the Motorola/IBM/Apple PowerPC, and Intel's Pentium. To be successful at these tasks, the LDO must provide plenty of "headroom."

While primarily designed to operate from input voltages between 3 and 5 V, the MIC5157 can handle input voltages as high as 36 V. It thus could be used to provide 12 V from a 15-V or higher supply rail. However, the MIC5157's output voltage, V_{out}, is fixed by pin-strapping to provide 12, 5, or 3.3 V. These voltages are set up by an internal resistor string, which is shown strapped to provide 3.3 V *(Fig. 1, again)*. Regardless of the input voltage, implementing the charge pump requires just a pair of small external capacitors (C_1 and C_2). The capacitor connected across the input improves the LDO's response



1. THE MIC5157 ENCLOSES A LOW ON-RESISTANCE power MOSFET within a negative-feedback, voltage-regulating control loop. It adds a voltage-tripling charge pump to power the error amplifier's output stage to create the FET's high-voltage gate-to-source drive. The gate must always be considerably more positive than its source, and often more positive than its drain.

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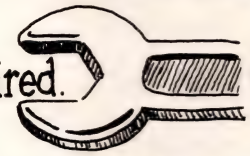
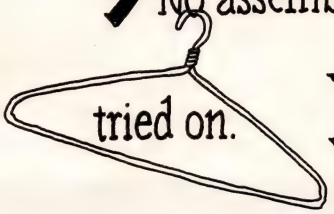
9 No assembly required.  8 They don't need to be tried on.  7 You can send them anywhere without having to pack them in big, brown boxes filled with .

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to input-voltage transients, while the capacitor connected across the load improves its transient response to load changes.

To give system designers more flexibility, the 14-pin MIC5157 is actually one of a trio of functionally similar ICs, the others being the 8-pin MIC5156 and the 14-pin MIC5158. The MIC5156 itself comes in four flavors. Following the path set by their IC regulator predecessors, both fixed- and adjustable-output versions are available. Thus, the basic MIC5156 has an adjustable-output voltage. An external divider lets users set it anywhere between 1.3 and 36 V. Alternatively, a potentiometer or multiplying DAC can be used to create a variable supply rail.

The MIC5156-3.3, MIC5156-5, and MIC5156-12, on the other hand, provide fixed-output voltages of 3.3, 5, and 12 V, respectively. In addition, all versions of the MIC5156 lack the charge pump. It's designed for systems that can provide an external high-voltage rail, such as the 12 V often required by mass storage, other peripherals, or analog circuitry. It could also be used with a p-channel MOSFET.

The MIC5158, like the MIC5157, contains a charge pump but it can only be pin-strapped to provide a 5-V output. However, like the MIC5156, an external divider sets any desired output voltage between 1.3 and 36 V.

Other features offered by these LDOs include current limiting, an Enable input, and an output "out-of-regulation" flag. Current limiting is implemented by inserting a current-sensing resistor in series with the input line and before the LDO regulator's drain pin. When the voltage drop across the user-selected current-sensing resistor exceeds 35 mV, the chip's current-limit comparator removes the power FET's drive. This shuts off the current to the load, thus protecting it and/or the FET. In addition, the output flag goes high (it also goes high if the output drops 6% below its nominal value).

With the Enable input at 0 V, the MIC5156/7/8 are in a sleep mode,

ALL ABOUT LDOs

Some define the dropout voltage of a linear regulator as the input-output voltage differential at which the circuit ceases to regulate against further input-voltage reductions. Micrel defines it as the input-to-output differential voltage that exists when the output drops to 99% of the nominal value it had with V_{out} + 1 V applied to the input.

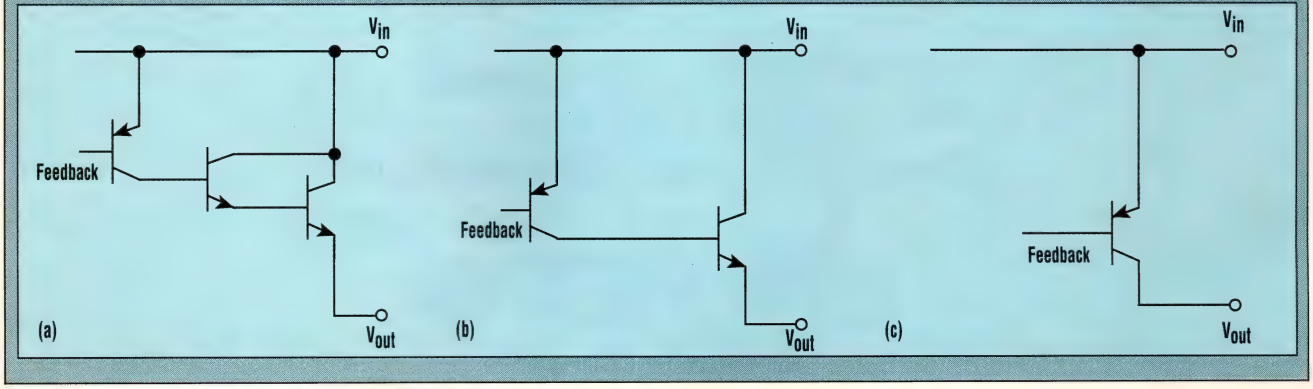
Classic IC linear regulators use Darlington-connected npn emitter-followers as pass transistors. At rated current, they typically drop out of regulation at 2.5 to 3 V *(see the figure, a)*. Moreover, these dropout voltages are still as large as 1.5 V at 1/10th the rated current. As a result, in most applications, the high power dissipation in high-current regulators (resulting from the product of current and high input-to-output voltage) creates the need for bulky heat sinks.

A typical IC using the circuit shown below might have a dropout voltage of 1.5 V at a current of 1 A, and a quiescent current (I_q) of 6 mA that doesn't flow into the load. However, all of the base current for the pass transistor flows into the load. Due to limited power dissipation with an input voltage of 30 V, the maximum permissible output current is just a mere 100 mA.

The first approach to reducing dropout voltage was to use the compound pnp/npn-transistor output stage *(see the figure, b)*. In these devices, dropout voltage at 1.5 A runs 1.5 V. However, I_q rises to 10 mA as the base current of the pnp transistor flows to ground, not into the load. Moreover, the output current for a 30-V input voltage drops to 75 mA.

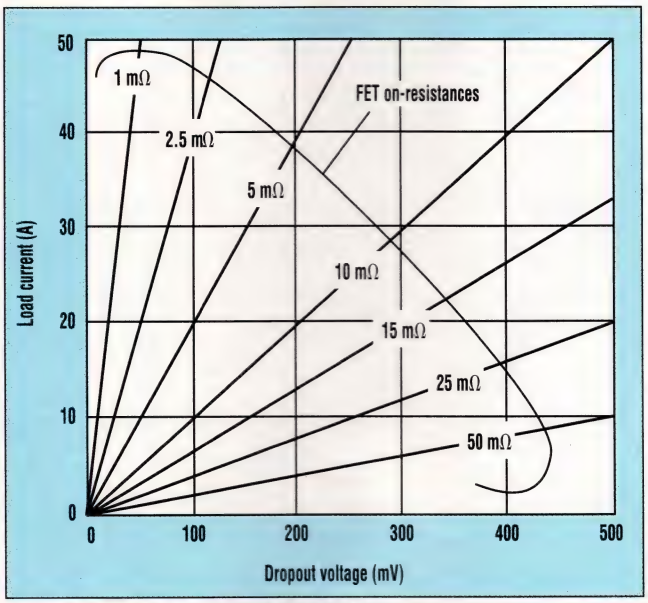
The next improvement in the LDO saw the use of the power-pnp-transistor output stage *(see the figure, c)*. Though the dropout voltage is down to 1 V at 1 A, none of the pnp transistor's base current goes to the load. The I_q runs 60 mA for 1 A of output current if the input voltage is 11 V. With a 6-V input, I_q climbs to 130 mA, but the output current for a 26-V input is now up to 1 A.

Replacing the power pnp transistor in the same circuit with Micrel's super-beta pnp device provides a dropout voltage of 300 mV at 1 A, but I_q is a mere 15 mA and output current at an input voltage of 30 V is still 1 A. Finally, the combination of the MIC5156/7/8 and a power MOSFET can provide an LDO with a quiescent current of 6 mA and no limit on the amount of maximum current or the minimum dropout voltage.



their quiescent current is typically just 500 nA, and the output is forced to 0 V. Bringing the Enable input to 5 V (while running off a 5-V rail) wakes them up when they're drawing just 6 mA], although they may be controlling 50 A or more.

A pair of circuits on the MIC5156/7/8 prevent the breakdown of the FET's gate-to-source oxide if its rated gate-to-source voltage (V_{gs}) is exceeded (the V_{gs} of many low-voltage, high-current DMOSFETs is 20 V, while that of most others is no more than 40 V). First, as noted earlier, the output of the charge pump is clamped to the input voltage V_{DD}, plus 16 V. If there's no V_{CP}-clamp circuit, the charge pump's output could be as much as 108 V if the input voltage is 36 V. Second, if the load is shorted, voltages as large as V_{DD} plus 16 V (potentially 36 + 16 V) can appear between the FET's gate and source. The 16-V Zener diode between the MIC5156/7/8's gate and source pins protects the FET from any gate-to-source overvoltage.



THE DROPOUT VOLTAGE of an LDO using an MIC5157 and a power MOSFET is simply the product of the load current and the on-resistance of the FET. Each line represents a particular on-resistance.

SUPER-β PNP PROCESS

First announced less than two years ago with a trio of ICs offering maximum current ratings of 250 mA, Micrel's super-beta pnp process creates monolithic LDOs with dropout voltages between 350 and 450 mV. The process now has been used to create a growing family of over two dozen LDOs, including several duals. Their capabilities span currents from a mere 100 mA to 7.5 A, and dropout voltages at rated currents run between 350 and 500 mV. At 5% of rated load, dropout voltage typically runs under 200 mV. And, at 0.1% of load, it can be under 50 mV.

Packages for family members range from tiny SOT-223s, SO-8s, and TO-92s, to three- and five-pin TO-220s and TO-263s (surface-mount tabless TO-220s), TO-247s, and two- and four-pin TO-3s. For example, the 150-mA MIC5200 drops out at 350 mV. It comes in fixed voltages (3.3, 4.5, 4.75, and 5 V) in SOT-223 and SO-8 packages with an Enable input. The MIC5202 is a 100-mA fixed-voltage dual that provides a similar dropout voltage in an SO-8 package with two Enable inputs. The 250-mA MIC2954 drops out at 450 mV. Fixed-voltage versions are available in TO-92, SOT-223, and 3-pin TO-220 packages. A full-featured version with Enable and Shutdown inputs and an output flag comes in 8-pin SO and DIP packages. In the latter package, the case acts as a 5th pin.

Rated at 400 mA with a 500-mV dropout, the MIC2920A through MIC29204 have fixed-voltage versions in SOT-223 and three-pin TO-220 packages, and full-featured devices in SO-8 and 5-pin TO-220 packages. The 1.25-A MIC2940A drops out at 450 mV and provides a fixed-voltage version in a 3-pin TO-220 package and a full-featured adjustable version in a 5-pin TO-220. Each full-featured 5-pin TO-220 has 3 versions offering two of the following features: an output flag, an Enable pin, and adjustability. The 8-pin devices offer all three features. The 1.5-, 3-, and 5-A units come in 3- and 5-pin TO-220s, while the 7.5-A LDOs come in the TO-247 case and two- and four-pin TO-3s.

Available three-pin devices provide fixed-output voltages offering some mix of the following voltages: 3, 3.3, 4.75, 5, 12, and 15 V. Additional pins are needed for the duals; in the singles they add such features as shutdown, adjustability, and an error flag. Output voltage of the adjustable LDOs can typically be set between 1.25 and 29 V with a pair of resistors or a potentiometer. Each family member provides fold-back current limiting, thermal shutdown, and can take automotive reverse-battery conditions (application of –20 V to the input). All but the 100-mA devices also can handle automotive "load dump" conditions at the input (a 60-V positive transient for less than 100 ms). The output flag flies high if the device goes out of regulation, then either goes into current limiting, shuts down due to overtemperature, or receives too many input load-dump transients.

Like all linear regulators using pnp pass transistors, the base current of the super-beta pnp transistor in these LDOs flows to ground rather than into the load, becoming the major part of the LDO's quiescent current, usually known as the ground current. The ground current is at its lowest just before dropout. It can vary from less than 0.1% of load current (at dropout) to over 10% (with maximum input-to-output voltage). During shutdown, ground current is typically less than 10 μA.□

PRICE AND AVAILABILITY

All plastic versions of the MIC5156/5157/5158 operate from –40 to +85°C. CERDIP versions of the MIC5156/5157/5158 and all Super-beta-based LDOs operate from –40 to +125°C. In quantities of 1000, the plastic MIC5156 goes for $1.31 each. The MIC5157/5158 in similar quantities go for $1.46 each. In lots of 1000, the price of the Super-beta-based LDOs ranges from $0.54 to $6.59, depending on package, configuration, and current rating.

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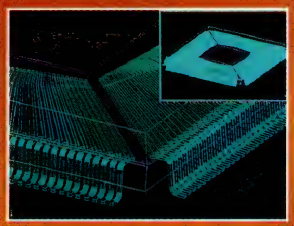

Courtesy of NCR Microelectronics

3 Choice of Extraction Methods

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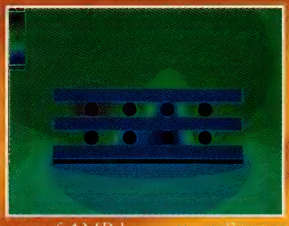
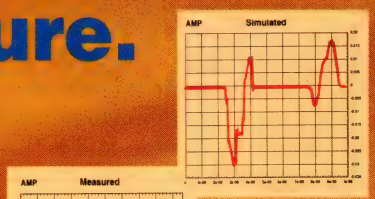
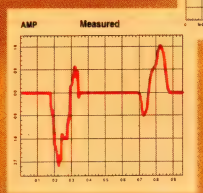


Courtesy of AMP Interconnect Systems





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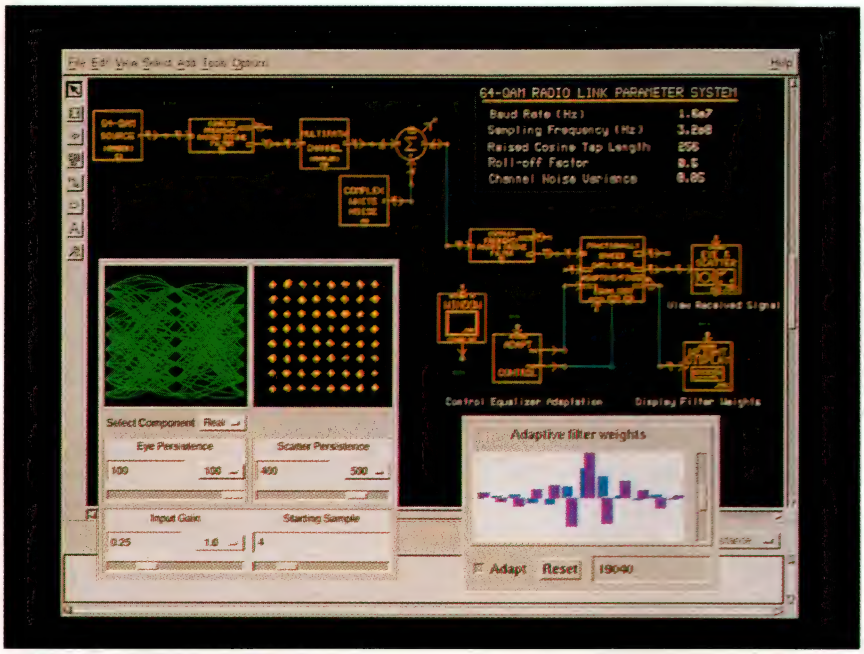

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EDA TOOLS ZERO IN ON DSP DESIGN

LISA MALINIAK

AUTOMATE DSP TASKS THAT SPAN ALGORITHM DEVELOPMENT TO PHYSICAL DESIGN.

The benefits of processing signals in the digital, rather than analog, domain are fueling the spread of digital-signal processing (DSP) into a growing variety of applications. But as more design teams are faced with creating DSP systems, the need for EDA tools to address that type of design becomes imperative. That's why many EDA vendors are responding with an assortment of specialized software, ranging from front-end algorithm development tools to back-end physical-implementation packages.

In addition to the array of point tools, several comprehensive design environments also are aimed at DSP design. These systems provide tools for all tasks engineers need to perform, as well as deliver them in a unified software environment that takes users from front to back in a smooth design flow.

To understand the advantages of the various DSP tools available today, it's important to first understand the different stages and overall flow of a typical DSP design. In fact, the comprehensive design systems developed by Cadis Software Ltd., South San Francisco, Calif.; Comdisco Systems Inc., Foster City, Calif.; and Mentor Graphics Corp., Wilsonville, Ore.; carefully address every step of a DSP design flow.

Basically, a DSP design begins as an algorithm aimed at accomplishing a particular signal-processing task. After an algorithm is created, it must be verified within the context of the entire system. Then, the algorithm can be implemented in software, hardware, or a combination of both. Engineers can opt for an off-the-shelf DSP processor, or move to ASICs and custom ICs. The latter route would obviously involve work with physical implementation.

The first step—algorithm design—can be divided into three stages. Most likely, three different groups of designers would work on these various stages, but they typically don't communicate among themselves. In the first stage, engineers create generic DSP algorithms, such as those for video compression or speech synthesis. This group usually consists of designers

with mathematical backgrounds who don't consider implementation issues. Their art is in designing the mathematical algorithm. In fact, they probably have no contact with the design group that performs implementation.

In the next stage, a design group will work to adapt these generic algorithms for a particular application. For example, a portable-telephone application might exploit speech compression and decompression algorithms. Therefore, engineers designing that portable telephone must look for algorithms that fit into the overall system design, and then fine-tune the algorithms for their application. There are many facets to fine-tuning, including defining the optimal buffer size for an existing algorithm. This design group probably needs a simulation environment where they can look at the overall system and the algorithm together, and perform tasks like changing algorithm parameters.

The third step of the algorithm design is fine-tuning the algorithm for a certain physical implementation. One example of the difficulty involved in this step comes from Herman Beke, general manager of Mentor's European Development Center (EDC), Leuven, Belgium. Beke, who is responsible for the company's DSP product, remembers a group of engineers who designed algorithms for a hearing-aid application. The group fine-tuned the algorithms only to find that they'd need a Cray computer to physically implement them. And, as Beke puts it, "it's tough to put a Cray computer in your ear."

The lesson is that although an algorithm may theoretically be perfect, it must be practical and be able to fit in a chip or on a board to be implemented. However, fine-tuning an algorithm to fit a given implementation takes a great deal of work. Engineers can optimize an algorithm to make it small, cheap, low power, or fast, all depending on the project's requirements. This represents the algorithm's final fine-tuning in an effort to obtain a certain implementation efficiency within an application.

Design automation is very important in these three stages of algorithm design. That's because all

1. THE BLOCK DIAGRAM editor in Cadis' Cossap DSP design system provides input to the stream-driven simulator, DSP-code generator, and VHDL-code generator. Also, the lower left of the screen shows the interactive signal monitors, which can be attached anywhere in the design without changing the block diagram.

three phases are done by different people. Generally speaking, designers with the ability to handle all three phases single-handedly are rare, if not nonexistent. Therefore, information transfer between the design groups becomes a significant bottleneck in DSP design. Despite the fact that the groups may fail to understand each other's work, they still must transfer information among themselves. This problem is most easily solved with EDA tools.

After the algorithm is designed and optimized, it must then be implemented in a system. This usually involves system-level simulation, which means engineers need VHDL models for parts of the system, including VHDL descriptions of the DSP blocks. Thus, it's helpful to have a design system that generates VHDL descriptions, starting with the algorithm description. A design system lacking that capability forces users to reenter the design with VHDL or some other design-entry method, slowing the design process and possibly introducing errors. It's best that the DSP design system doesn't require users to reenter the design at every phase. They should be able to enter the design once, and then be able to automatically generate the subsequent versions.

Once the overall system is simulated and working, the design is handed off to the physical-implementation designers. For DSP design, this stage typically involves real-time emulation. For example, if the DSP design is a CD player, real-time emulation would allow a design team to actually hear how the product will sound before it goes to production. In fact, there may be many different algorithm implementations, and listening is the acid test that determines which one sounds best. Therefore, the next step is to build a prototype for real-time emulation.

For fast prototyping, most engineers choose an existing DSP processor, which can be purchased alone or on a board. For instance, several board vendors offer products incorporating Texas Instruments' C40 digital signal processor. Such products allow design teams to verify the system in a real-life environment.

After a working prototype is built, the design team pursues a production-style implementation. The first crack at such an implementation

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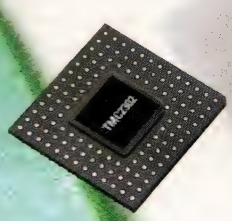

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TMC 22x5x Digital video decoders	3-line comb filter	8 and 10 bits	10 to 18 Mhz
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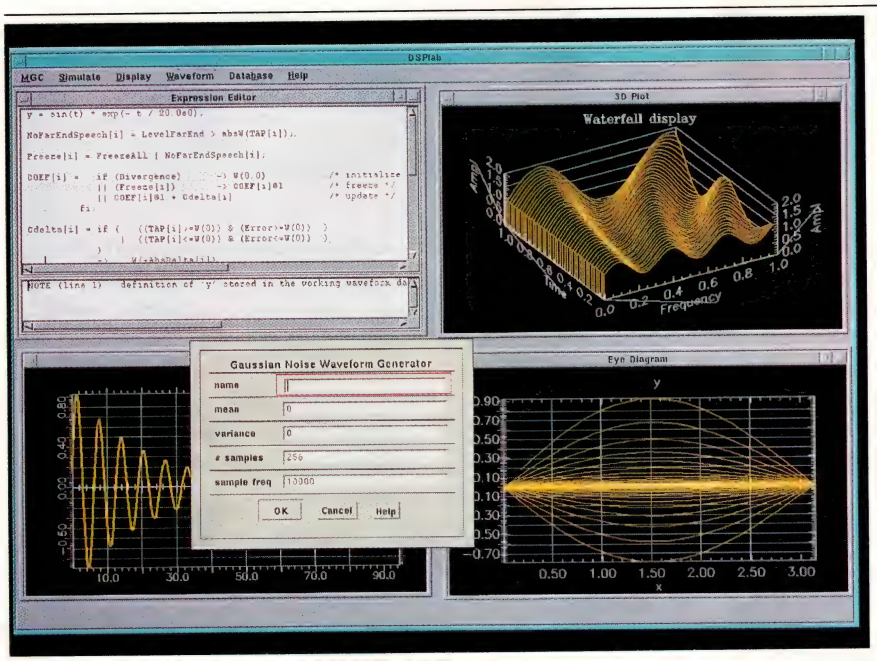


2. ENGINEERS CAN SIMULATE designs in both the time and frequency domains with the DSP Station software developed by Mentor Graphics. The expression editor shown in this screenshot defines or processes signals through a combination of mathematical expressions and a high-level DSP-specification language.

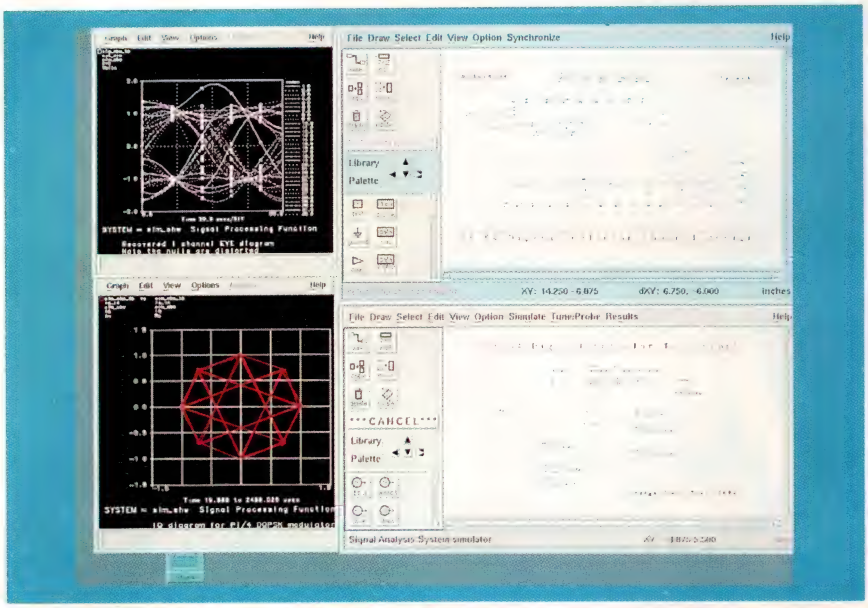
might be centered on a gate array. The next generation of the processor may be a full-custom IC if much higher volume is demanded. Today, the best way to solve this ASIC-implementation problem is to produce a VHDL description of the architecture (RTL description), and then to go into logic synthesis or module generation for implementation.

For full-custom implementation, the design team needs an IC-design environment. First, they must come up with an overall architecture to implement the DSP system. This becomes yet another bottleneck in DSP design. That's because engineers may want to optimize the chip for speed, power, or area, and it's not obvious which architecture will yield the best result. Moreover, few tools exist that allow engineers to do architectural design exploration. Users thus need a way to quickly evaluate four or five different architectures to determine the best one.

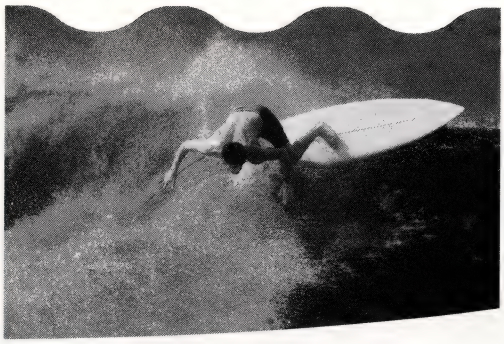
Because engineers will typically go through all of three of these implementation stages during the life of a product, design tools should not only support all three but should also have interfaces between them. For instance, engineers may use a standard processor for low-volume applications, a gate array or standard cell for medium volumes, or a full-custom IC for high volumes. In many cases, though, they will actually go through all of these steps, and a good DSP design environment will minimize the time and effort involved in moving through them. Doing so involves supporting both hardware and software design. That's because when a prototype is based on a standard processor, the design effort is concentrated in software development, not hardware design. A custom IC, on the other hand, requires heavy-duty hardware design.

One newer design bottleneck involves hardware-software co-design. For example, hardware-software co-design is important for a design option called the embedded-core chip, which falls between the standard DSP processor and the full-custom IC or ASIC. The embedded-core chip is similar to the embedded microprocessor chip, except that it has a DSP core as a standard cell for engineers to design the logic around. What typically happens is that engineers put part of the algorithm in the core, which they program with software, and part in hardware (gates). To create the hardware, they generate VHDL descriptions and perform logic synthesis. Consequently, the design team must do hardware and software design together. This particular design problem has yet to be adequately addressed by existing DSP environments.

All three comprehensive design



3. A DIGITAL CELLULAR RADIO is a good application for HP EEsof's Communications Design Suite. The schematic window in the upper right of the screen is used to enter the design. In the Test Bench window in the lower right, the completed design is connected to icons representing laboratory measurements. The results of two of these simulated measurements—an eye diagram and a constellation diagram—are shown in windows on the left of the screen.



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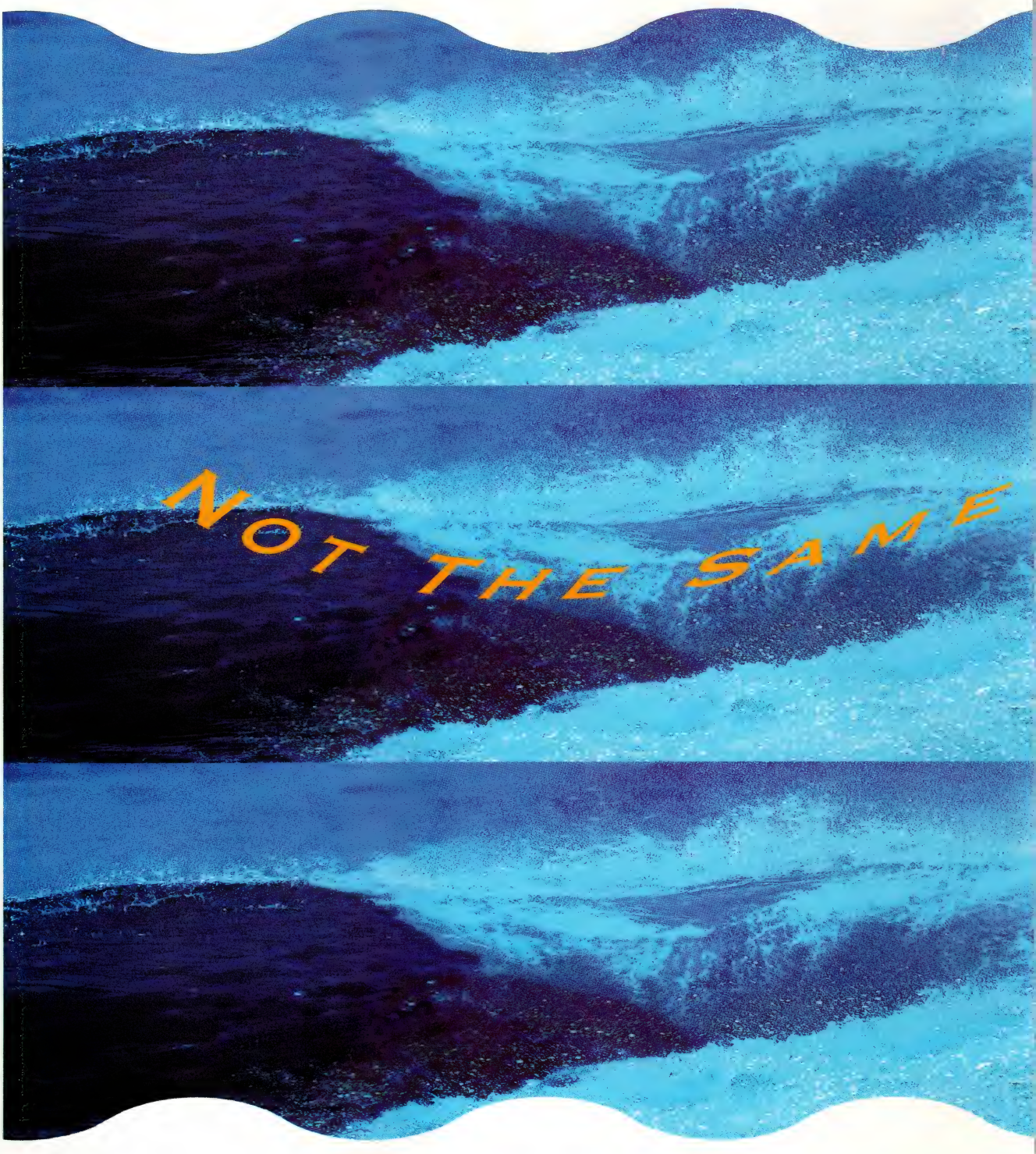

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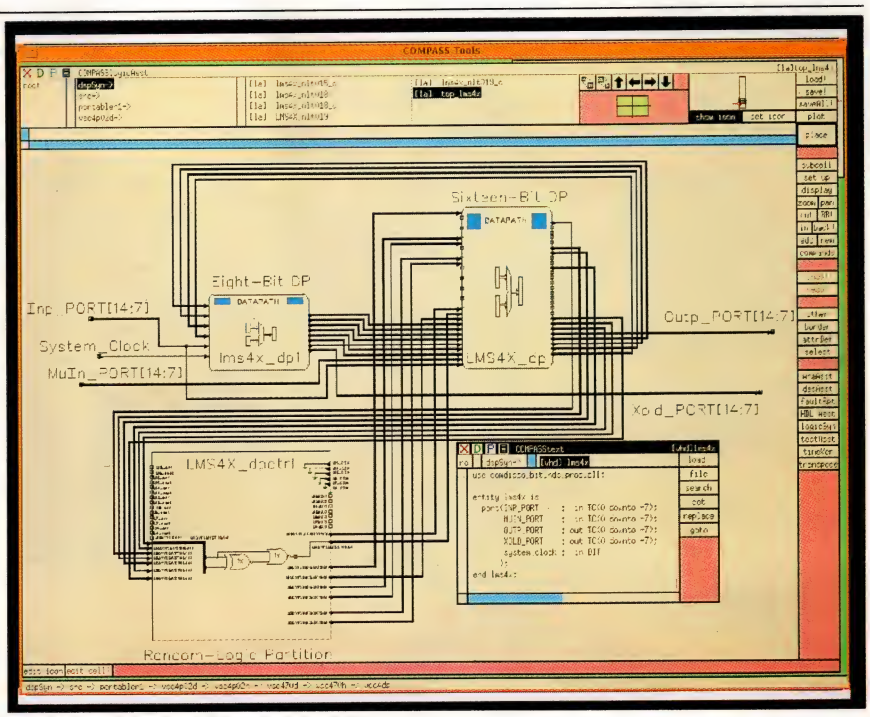
environments (from Cadis Software, Comdisco Systems, and Mentor Graphics) do a good job of addressing the needs and bottlenecks of the DSP design cycle. Cadis' system, called Cossap, combines design, simulation, and implementation in one environment *(Fig. 1)*. A conceptual system is defined by drawing its block diagram on the screen, and then assigning values to the parameters of the blocks. The blocks include such functions as codecs, modems, and filters. Each block diagram is stored as a VHDL net list.

After entry of a number of conceptual systems, the most promising ones can be studied in greater detail. With Cossap, users can analyze the effects of implementation-related issues, such as finite word length. Engineers refine the system until they have an accurate bit-level representation of their design. Cossap supports this step by providing a library of blocks for specifying and executing algorithms at the bit level.

Once a system is settled upon, it's then verified with the Cossap stream-driven simulator. The stream-driven approach will simulate any system whose inputs and outputs can be modeled as a sequence of values. That includes designs incorporating multiple sampling rates, and mixed time- and frequency-domain processing.

The next step is to implement the system. For programmable digital-signal processors, the Cossap DSP Code Generator automatically generates software from the graphical block diagram. For a hardware implementation in an ASIC or FPGA, engineers use the VHDL files from the block diagrams as input to a synthesis tool.

Comdisco's complete design environment, called DSP Framework, combines core technology from the company's Signal Processing WorkSystem (SPW) with capabilities targeted at DSP design *(see the opening photo)*. SPW is a graphical environment for system-level design, simulation, and implementation of either hardware- or software-based DSP and communications systems. The additional capabilities include an intuitive user interface, system-level block-diagram-based design, signal manipulation, filter design, and an open database.



4. FOR DSP ASIC DESIGN, the tools created by Compass Design Automation partition high-level descriptions into datapath and control logic. Users can synthesize either an optimized layout through the company's Datapath Compiler, or a gate-level net list. The Compass tools are integrated with the Comdisco DSP tools, and support a comprehensive DSP behavioral library. This example shows a parametrized, datapath bit-slice schematic with random logic that's been synthesized from a Comdisco VHDL description.

Engineers can enter their signal-processing designs with text or graphics at the behavioral and architectural levels. The behavioral level is specified by signal-flow block diagrams. Architectural-level design graphically specifies and automatically synthesizes DSP ASICs and FPGAs.

With DSP Framework, designs are partitioned for implementation in hardware and software. SPW converts the design into C or assembly code for software implementation. This includes code for single or multiple processors. On the hardware side, SPW converts a design into synthesizable VHDL for implementation in an ASIC.

SPW has a fast behavioral simulator that supports real-time interaction with the design by means of "virtual human interfaces." Simulations can be executed on the workstation or downloaded to a mainframe or a DSP-development system. Real-time software prototypes of the design are possible when targeting a DSP development system through on-board analog-to-digital and digital-to-analog converters.

The DSP Station developed by Mentor Graphics is a top-down design environment for DSP design and synthesis that lets users create both hardware and software implementations *(Fig. 2)*. DSP Station consists of the Design Architect schematic and textual capture tool and symbol editor, as well as the DSP Architect DSP-specific simulation and analysis environment. Options include a filter-design package, VHDL-generation capabilities, and Mistral architectural synthesis tools.

With DSP Station, users are able to start with a generic algorithm design. Engineers can enter their algorithm in three different ways: using a schematic editor combined with special libraries; employing a text editor equipped with a special language called Dataflow Language (DFL) that's ideally suited for describing DSP systems; and using the C language for simulation and algorithm optimization. Much previous

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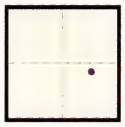

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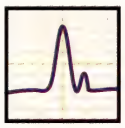

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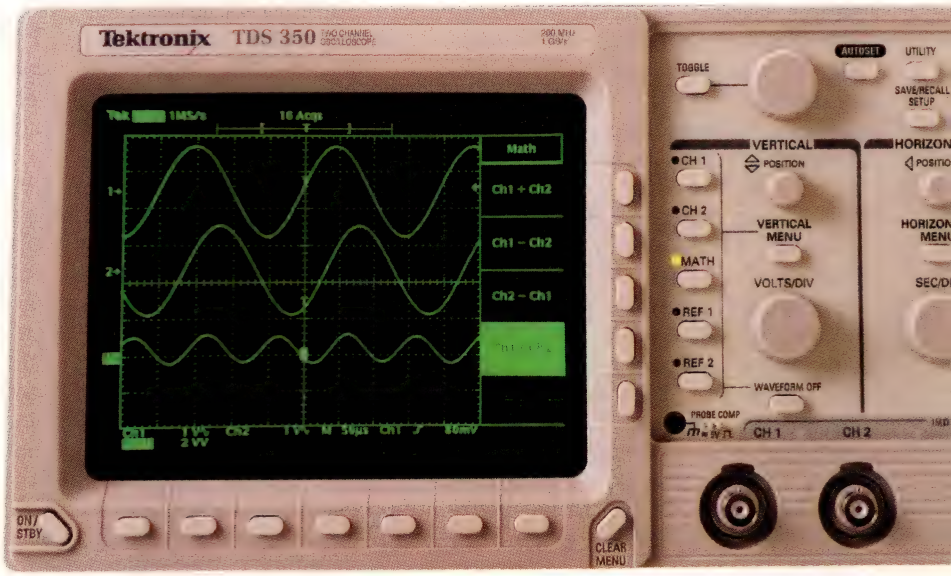

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Channels	2	2	2
Vertical Sensitivity	2 mV - 10 V	2 mV - 10 V	2 mV - 10 V
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READER SERVICE 109

DSP work has been done with C.

Engineers simulate their algorithm with the fast, frequency-domain simulator in DSP Architect. In addition, DSP Station helps users fine-tune their algorithms for certain applications. For example, the company's telecommunications simulation library is used with the DSP simulation environment to help users create communications algorithms. Mentor is currently working on a similar package for video applications, and envisions having others available in the future.

Mentor Graphics just began to address the hardware-software co-design issues. In DSP Station, users creating an algorithm don't have to know if it will be implemented in hardware or software because the description method is the same either way. DSP Station also supports both software and hardware implementation. On the software side, the system can generate C code for any standard DSP processor that supports a C compiler, as well as generate assembly code. On the hardware side, the Mentor tools can feed the design description to the company's Mistral 2 software, which can synthesize a DSP architecture, datapath, and controller. It has predefined VHDL library elements (synthesizable VHDL) that can be fed to standard logic synthesis to create a gate-level design.

In addition to these front-to-back DSP design environments, a number of point tools can tackle specific tasks in the design flow. Tools from companies like The MathWorks Inc., Natick, Mass.; and MathSoft Inc., Cambridge, Mass., help engineers come up with the mathematical algorithms that are required at the beginning of the DSP design process. MathWorks produces Matlab, a technical computing environment that features various application-specific Toolboxes. The Signal Processing Toolbox is a collection of functions for one- and two-dimensional signal processing. The central features of the package are functions that implement digital filtering and power-spectrum estimation (fast-Fourier-transform) techniques.

MathSoft also has a signal-processing option for its Mathcad numerical calculation software. Called the Signal Processing Function Pack, it's a collection of more than 60 signal-processing functions used in DSP systems. Some of the package's capabilities include spectral analysis, transform analysis, digital filtering, and filter design.

For communications-specific DSP design, HP EEsof, Westlake Village, Calif., offers a Communications Design Suite for its Series IV high-frequency design tools *(Fig. 3)*. The Communications Design Suite contains libraries that allow engineers to analyze the effects of a DSP element in its target system.

HP EEsof also offers the DSP Network Test Bench, which tailors the company's discrete-time simulator to design functions or algorithms composed solely of DSP elements that process a baseband signal. Within a network of these elements, designers can analyze both real and imaginary numbers. Users can simulate a wide range of DSP functions, including Viterbi decoders. Once the design and simulation of the DSP network is finished, it can be placed in a complete system schematic for overall analysis. The test bench can also output SPW files for use with Comdisco's tools.

Rapid prototyping of DSP designs is possible with the Paradigm RP system developed by Zycad Corp., Fremont, Calif. Paradigm RP can accommodate the near-real-time testing of digital signal processors with complexities up to and beyond 120,000 gates, and with clock speeds exceeding 10 MHz. The system is based on a 30,000-gate module made up of FPGAs. A graphical user interface lets engineers import, partition, and map DSP designs to the system's emulation hardware. Zycad will support a range of plug-in submodules covering most of the standard DSP devices.

To create DSP hardware, the DSP Design Option from Compass Design Automation Inc., San Jose, Calif., provides the critical link between system-level design and chip implementation. Engineers enter a design using a system-level DSP design and analysis tool. Compass also provides a direct link to the Comdisco tool. DSP Design Option can read a behavioral VHDL specification, and then automatically generate hierarchical datapaths and random-logic schematics. The company's Datapath Compiler software creates optimized-layout datapath blocks that are smaller and denser than most manually created layouts *(Fig. 4)*. In addition, the DSP library available with the Compass tools contains a wide selection of elements, including adders and multipliers.

Many DSP designs are eventually implemented in software on an off-the-shelf digital signal processor. If a design is going that route, each of the DSP chip vendors possesses its own development system. For example, the development system from Texas Instruments, Dallas, supports users from concept to production. The TI system helps at the conceptual level with application notes, users' guides, and technical support hotlines. Engineers can then evaluate their ideas with an assortment of evaluation models, simulators, assemblers, linkers, and compilers. These tools help gauge the processor's performance, benchmark time-critical code, and determine the feasibility of using one or multiple devices. Then, software and hardware design is completed, and all sections of the system are integrated for final verification.

Development tools from Hyperception Inc., Dallas, Texas, support most of the DSP chips and boards that are available. Their most popular product is HyperSignal for Windows Block Diagram, which lets DSP engineers design algorithms graphically, execute them in real time on a plug-in DSP board, and generate C code for the algorithm. Users arrange and connect signal-processing blocks to design, adjust, and test DSP algorithms. Parameters are adjusted by clicking on blocks and entering data on a pop-up menu. An optional C source-code generator produces the code for a block diagram that can be cross-compiled for a particular DSP chip.□

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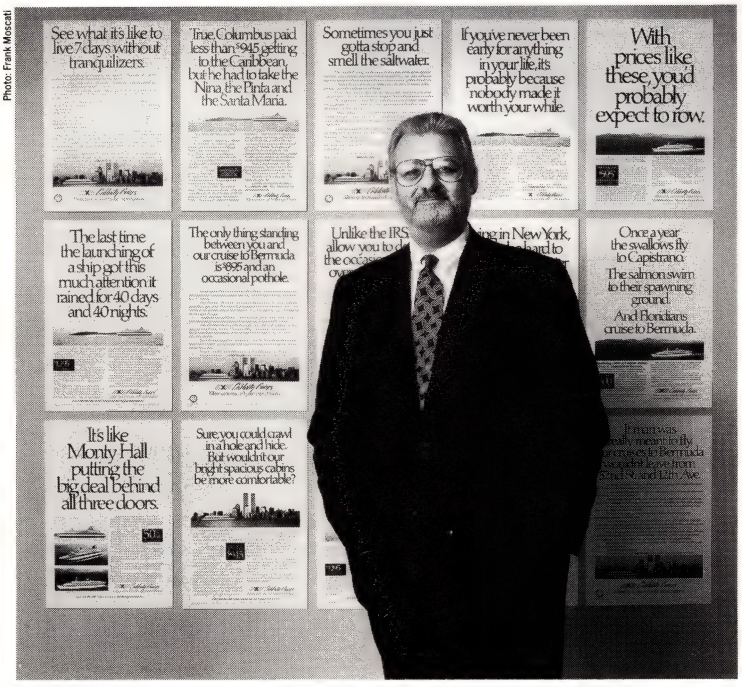
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Photo: Frank Moscati

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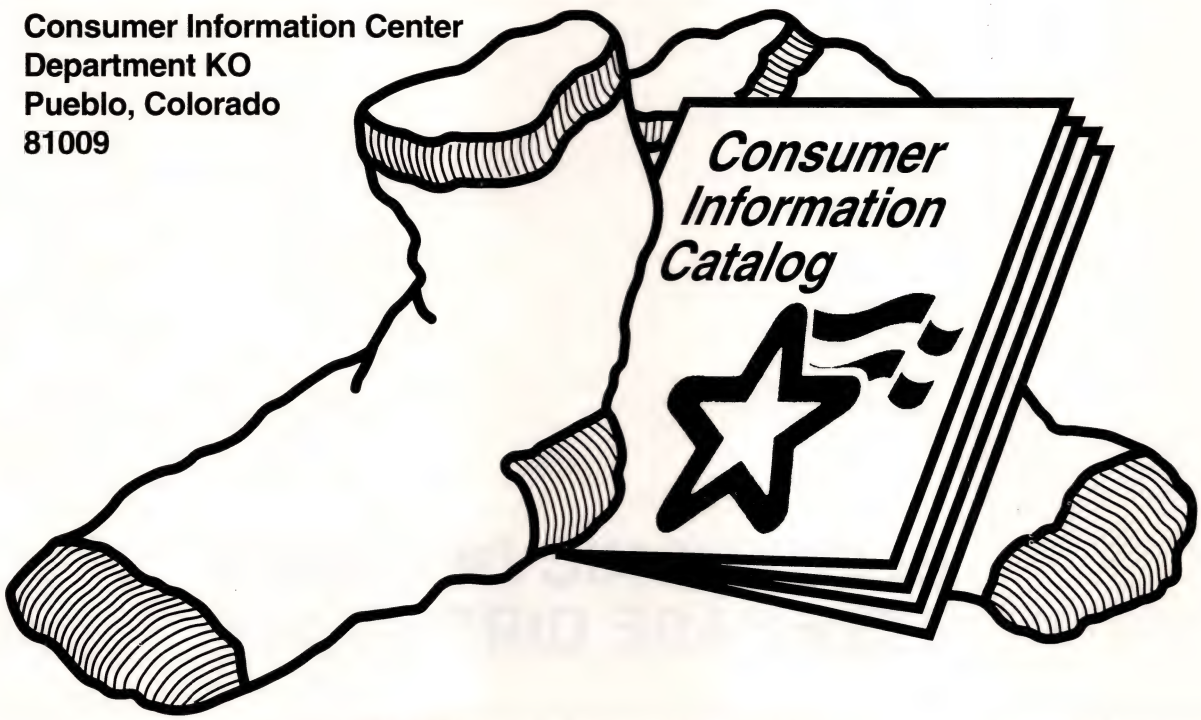

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LOW-VOLTAGE-SWING CMOS DRIVES 100-MHz BUS

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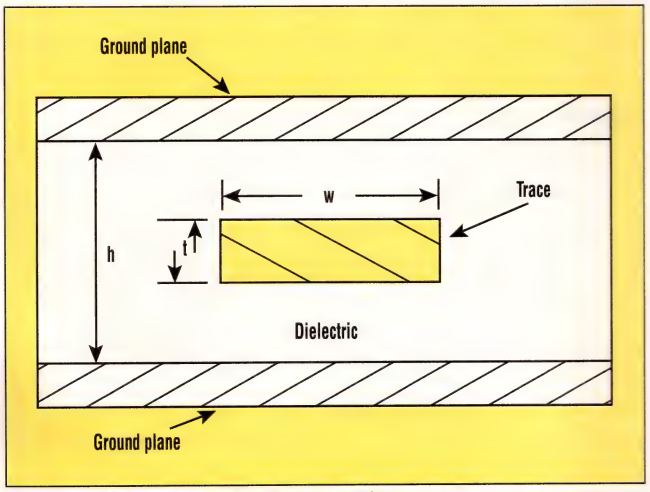
Blazing processor speeds have created a data bottleneck on processors and I/O buses, as data-transfer demands exceed the capabilities of the buses. Indeed, system interconnects with data bandwidths near 100 MHz are needed to keep pace with the requirements of the computing marketplace. However, increasing the clock frequency on a multidrop bus causes transmission problems for board and chip designers. Another point to consider is that the higher speeds exceed the bus bandwidth limits of full-swing TTL and CMOS signals. These levels, minimum 2-V swings with uncontrolled transition slew rates, make designing high-frequency circuit boards very difficult.

Of course, familiar design guidelines—short stubs and signal paths, controlled impedance, and matching terminations—help to extend the life of the old signalling technology. But the practical limits have been reached, so new bus architectures and signal types are being introduced. The local bus approach, in the form of PCI and VL buses, uses traditional signal levels and fine tunes the bus to squeeze out the maximum performance. Even so, these buses have difficulty linking directly to a high-frequency processor because of their bandwidth, less than 50 MHz.

Fortunately, a new signal standard nearing completion, low-voltage-swing (LVS) CMOS, will deliver bus-to-chip and chip-to-chip bandwidths of 100 MHz. The low signal swing allows fast switching rates in the proper transmission-line environment. This article describes the design of an appropriate bus.

LVS CMOS, commonly referred to as Gunning transceiver logic (GTL), was conceived to allow transceiver integration onto VLSI and ASIC parts, thereby eliminating the need for discrete transceivers. Integration is possible because of the low power dissipation of the chip's transceivers. The standard specifies an open-drain driver output that's pulled up to a termination voltage of 1.2 V *(see "How low-voltage-swing CMOS Works," p. 68).* The specified output voltage low is a maximum of 0.4 V at 40 mA sink current. That creates a maximum dissipation of only 16 mW per channel.

The dc voltage-level standard is fine for digital interoperability, but it doesn't account for transmission-line effects. To ensure proper operation, the ac parameters of



1. THE CHARACTERISTIC impedance of a stripline pc-board trace depends on its physical dimensions and the dielectric constant. For low-voltage-swing CMOS, the loaded bus impedance should be at least 50 Ω.

100-MHZ BUS DESIGN

high-frequency switching and fast slew rates should be considered. The performance and noise design issues must be addressed using transmission-line techniques.

The best way to ensure that a bus will reach a bandwidth of 50 MHz or more is to guarantee incident-edge switching. Incident-edge switching means that the initial change in voltage states passes through the receiver threshold with a reliable noise margin. There's little if any ringing caused by reflections that pass the signal back to the receiver threshold region. In some buses, this ringing is referred to as settling time, which is the time it takes for reflections and crosstalk to subside. Settling time slows bus throughput by requiring extra set up time at the receiver. It's the price that the user pays for an improper bus design.

To create incident-edge switching, the designer calculates the loaded-bus impedance and terminates the bus ends with this impedance. As a result, the energy in the incident wave is absorbed rather than reflected back into the bus, where it would cause noise problems. This relationship is expressed by the reflection coefficient equation:

$$\rho = \frac{Z_{term} - Z_L}{Z_{term} + Z_L} \quad (1)$$

where ρ is the reflection coefficient, Z_{term} is the termination resistor, and Z_L is the loaded impedance of the bus. The loaded impedance and terminating resistors will then determine the amount of current needed to push incident edges through the receiver threshold with enough noise margin to ensure reliable data transfers.

A GTL bus design begins with the integrated transceivers' ac specifications for slew rate and I/O load capacitance. Although the LVS CMOS standard doesn't specify them, they're important to performance.

The slew rate is critical when specifying controlled-impedance signal paths. The slower the slew rate, the more forgiving the signals are to impedance mismatch problems caused by stubs, vias, and connectors. The parasitic output loading capacitance of inactive drivers on the bus is crucial when designing for the proper loaded impedance. The loaded-bus impedance determines the matching

HOW LOW-VOLTAGE-SWING CMOS WORKS

Low-voltage-swing CMOS uses the active pull-down and passive pull-up technique to change bus voltage levels. The driver is an open-drain transistor that's pulled up to a termination voltage, V_{tt}, through a termination resistor *(Fig. A)*. V_{tt} is nominally 1.2 V, and the termination resistor is specified at 50 Ω. When the bus is terminated at each end, the dc load is 25 Ω. Maximum V_{ol} is 0.4 V while sinking 40 mA of current.

The receiver is a high-speed comparator. Because the minimum voltage swing is only 0.8 V, the receiver threshold must be very tight to ensure adequate noise margins. In LVS CMOS, a receiver threshold of 0.1 V is possible by controlling the threshold reference voltage. The resulting 0.35-V noise margins are very good *(Fig. B)*. A resistor-divider network from the termination voltage supplies the threshold reference. The LVS CMOS standard specifies the threshold as 2/3 V_{tt}. This reference will track with variations in termination voltage. The ±50-mV tolerance allowed is very tight for a receiver but is essential for maintaining the noise margin.

LVS CMOS's major advantage is lower power dissipation. This benefit results from the reduced V_{ol} and sink current. The logic-low output voltage of 0.4 V at 40 mA translates to a maximum power on chip of 16 mW per channel. This is the worst-case power condition on the bus, because no current is being sunk in the logic-high state.

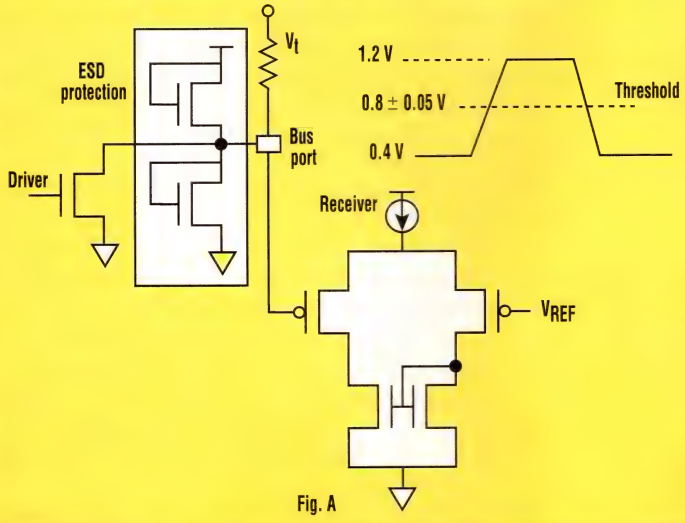


Fig. A

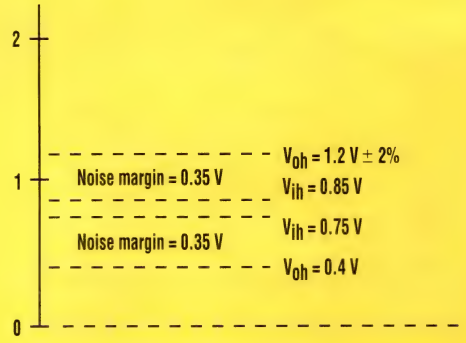
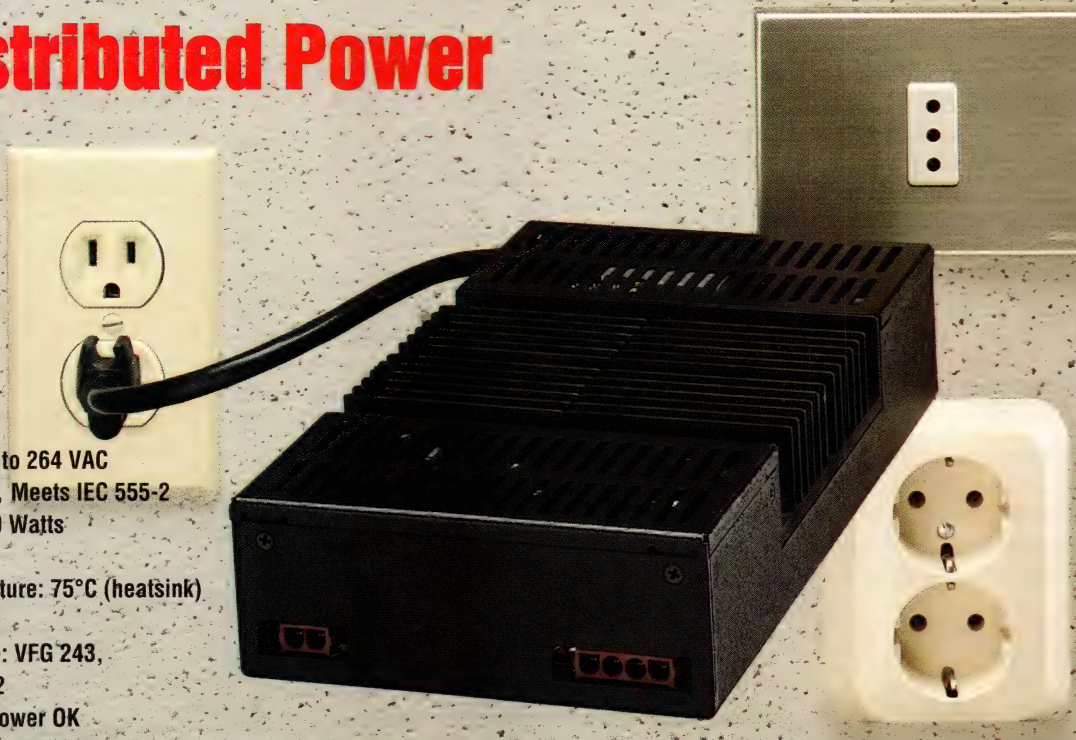


Fig. B

HAMPAC™

Universal Input
Unity Power Factor Front End
For Distributed Power

1200 Watts
Power Factor Corrected



- Universal Input: 85 to 264 VAC
- Unity Power Factor, Meets IEC 555-2
- Output Power: 1200 Watts @ 260-425 VDC
- Operating Temperature: 75°C (heatsink)
- Efficiency: 90-94%
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- Module Enable & Power OK
- Auxiliary Supply 12 VDC @ 10 mA
- Active Output Voltage Control
- Input Transient Protection
- UL, CSA, TÜV (in process)
- Inrush Limiting <20 Amps Peak at 115 VAC
- Size: 10" x 5.25" x 2"

Vicor's HAMPAC...an economical, off-line, universal AC input, power factor corrected front end...delivers 1200 watts of output power in a low profile, chassis-mount housing.

The HAMPAC interfaces directly with worldwide AC mains and delivers a DC output to power Vicor's isolated, high density VI-26X and J6X families of DC to DC converters. Additionally, the HAMPAC provides line rectification, EMI/RFI filtering, transient protection, inrush limiting and holdup. No matter what your requirements...no matter where in the world... Vicor has your front end — the 10" x 5.25" x 2" HAMPAC.

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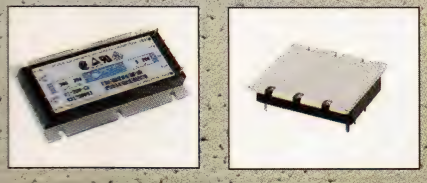

VI-26X and VI-J6X DC-DC Converters, compatible with the HAMPAC.

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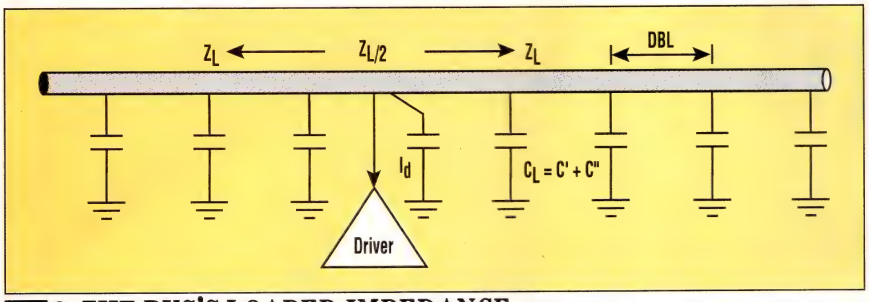


2. THE BUS'S LOADED IMPEDANCE, Z_L, depends on the distributed load capacitance per load, C_L, which includes C', the capacitance of vias and connectors (typically 1.5 pF per load), and C'', the transceiver output capacitance (typically 12 pF per load).

termination resistor value and thus the amount of current the driving transistor must sink.

The LVS CMOS standard specifies a 50-Ω load. In practice, this means that the loaded-bus impedance (Z_L) should be at least 50 Ω. The characteristic impedance (Z_o) of a stripline pc-board trace depends on its dimensions and the dielectric constant:

$$Z_o = \left(\frac{60}{\sqrt{\varepsilon_r}}\right) \ln\left[\frac{4h}{0.67\pi\,(0.8w+t)}\right] \quad (2)$$

where ϵ_r is the relative dielectric constant, h is the height between ground planes, w is the trace width, and t is the trace thickness *(Fig. 1)*. Z_o can also be expressed as:

$$Z_o = \sqrt{\frac{L_o}{C_o}} \quad (3)$$

where L_o and C_o are the characteristic inductance and capacitance. A typical Z_o is 75 Ω.

This bus can be loaded evenly to achieve the 50-Ω loaded impedance. The loaded impedance is given by:

$$Z_L = \frac{Z_o}{\sqrt{1+\frac{C_L}{C_o}}} \quad (4)$$

where C_L is the distributed load capacitance per load *(Fig. 2)*. C_o is typically 125 pF/m for the 75-Ω trace. C_L is the sum of the parasitic capacitance of connectors, vias, and the pc-board stub (C'), and the transceiver output capacitance (C''). The latter is the capacitance of the inactive driver, receiver input, ESD protection parasitic, leadframe, and package.

The required distance between the loads (DBL) is:

$$DBL = \frac{C_L \text{ per load}}{C_o\left[\left(\frac{Z_o}{Z_L}\right)^2 - 1\right]} \quad (5)$$

With typical values of 3 pF for the connectors, via, and stub, and 9 pF for the transceiver output capacitance, the capacitance per load is 12 pF. For C_o = 125 pF/m and 50-Ω loading, the loads must be 76 mm apart. As a result, 10 loads would require a bus approximately 0.75 m long.

A bus this long would delay signal propagation to logical devices. Consequently, minimizing the transceiver load capacitance and stub parasitic capacitance are very important in high-frequency bus design. Designers must eliminate vias and connectors wherever possible and limit transceiver load capacitance to less than 4 pF total at the pin.

With a C_L of 6 pF rather than 12 pF, loads could be spaced at a more reasonable 38 mm (about 1.5 in.), half the distance calculated previously. The propagation speed through 38 mm of 75-Ω trace is about 240 ps, so the delay between each load on the bus would be less than the transition time. Consequently, the designer can treat the bus like a uniform transmission line of 50-Ω characteristic impedance.

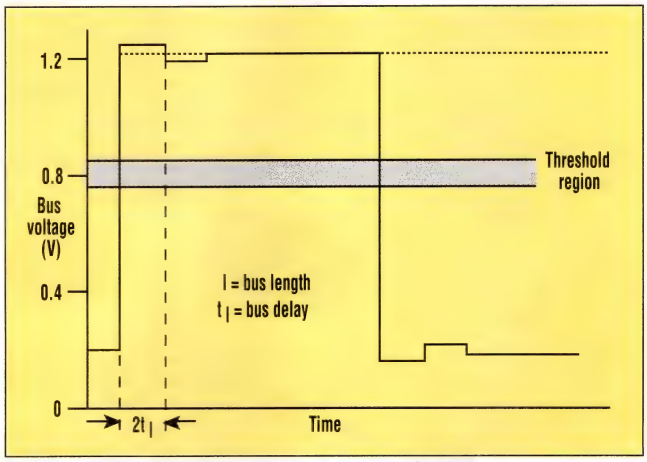
This 50-Ω impedance will offer a 25-Ω load to the incident edge of a signal driven from the bus center. The incident voltage step can be calculated by multiplying the current by the initial impedance seen by the driver output. For GTL, 40 mA multiplied by 25 Ω produces the 1 V needed to drive the signal from 1.2 V to 0.2 V on the first voltage step *(Fig. 3)*. This allows for the full voltage swing plus noise margin. Thus, incident-edge switching can be achieved by limiting the load capacitance, matching the termination to the fully loaded impedance, and having enough drive current to produce the full voltage swing from any drive position.

Another advantage of reduced load capacitance is increased bus speed. Intuitively, the greater the load, the more time spent charging that load. Mathematically, the relationship between loading and propagation delay is:

$$t_l = l(t)\sqrt{1+\frac{c''+c'}{c_o}} \quad (6)$$

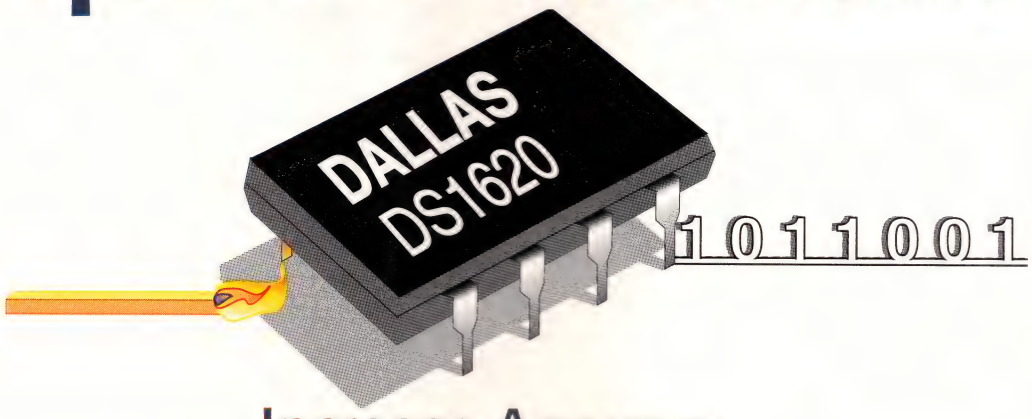
where t_l is the loaded propagation delay, t is the unloaded propagation delay, and l is bus length. C_o, C', and C'' are defined as before. Typical GTL values are l = 342 mm; t = 7 ns; C_o = 125 pF/m; C' = 1.5 pF/38 mm; and C'' = 6.0 pF/38 mm. For these values, t_l = 3.8 ns. The total throughput depends on bus delay. Because a long bus must be enhanced in any way possible, increasing bus propagation speed becomes important to increasing the total throughput.

Transition times are very important to high-performance bus design. Since it's independent of voltage lev-



3. THE INCIDENT VOLTAGE STEP is developed by the driver current of 40 mA multiplied by the initial impedance seen by the driver, which is 25 Ω at the bus center.

Direct-to-Digital Temperature Measurement



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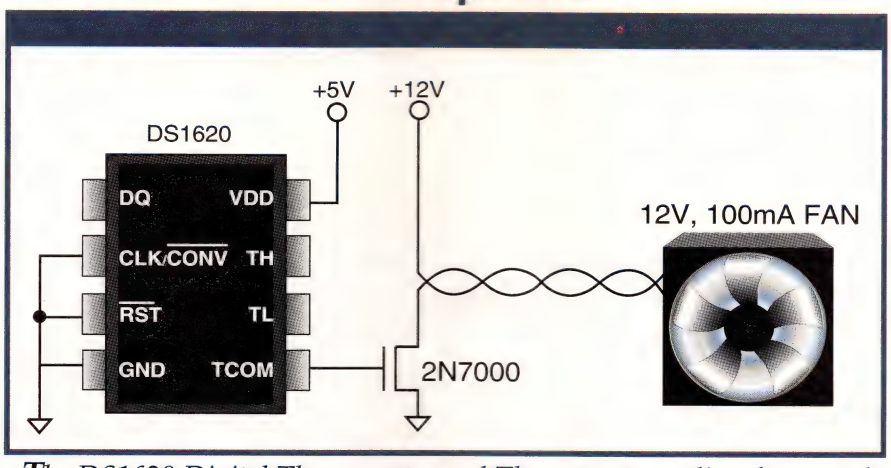

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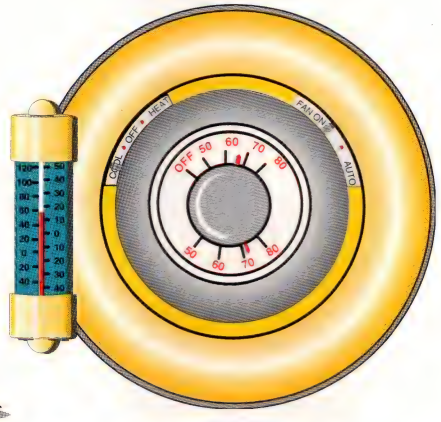

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READER SERVICE 144

el, slew rate can best specify the transition time characteristic. Slew rate and voltage swing are responsible for the intensity of the electromagnetic field that accompanies the propagating signal. This field induces signals on nearby conductors, resulting in crosstalk.

By lowering the voltage swing to 1 V, LVS CMOS reduces the crosstalk problem. Slew rate should also be as low as possible while still meeting the minimum sample window size at the receiver input. The optimum way to measure slew rate for GTL is between fixed voltage levels, which eliminates test fixture variations. A good range is 0.5 V to 1 V, because it does away with the overshoot and undershoot variations that can be uniformly tested by the IC manufacturer.

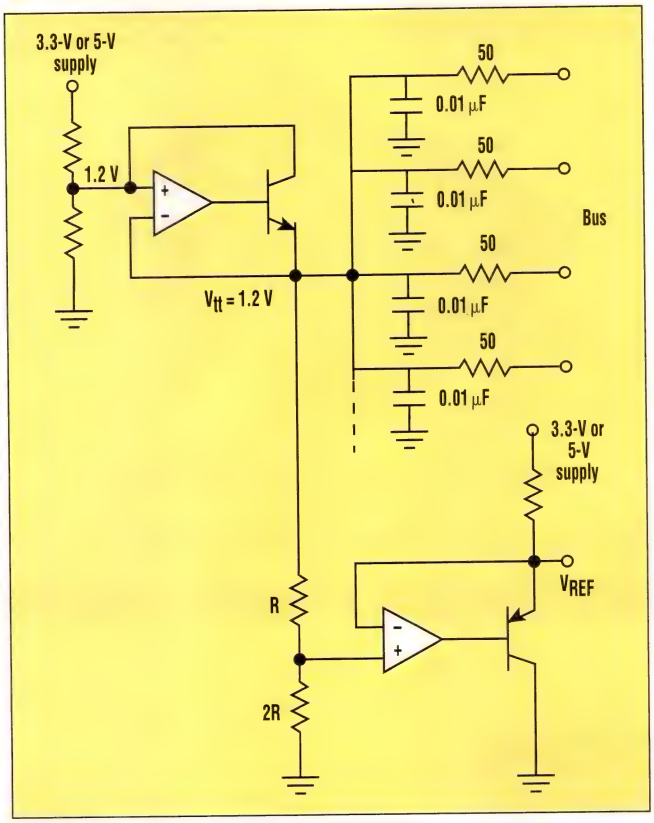
If 625 ps is specified as the minimum time in which the transition can be made, the slew rate would be 0.8 V/ns. If the full transition time is about double that, or 1.2 ns, it would be 24% of the bit width at 100 MHz (or 5 ns). This should leave an adequate sample window.

Along with slew rate, stub length is another interactive parameter that the board designer must analyze closely. Stub length is the distance that each load is removed from the direct bus path. The stub signal path includes connectors, vias, pc-board trace, and IC pin solder pads. These varying components usually create an impedance discontinuity between the stub and the bus. The stub is only terminated at the high-impedance receiver input. Therefore, the reflection coefficient on the stub is nearly one, and the incident wave is reflected completely from the receiver input.

To avoid noise problems, the amplitude of the reflected energy must be small. If the stub's electrical distance is greater than 1/5 of the transition time, reflections of greater than 20% of the energy from the incident wave will cause ringing noise on the stub. With a transition time of 1 ns, an electrical distance greater than 200 ps will create significant reflections. Typically, this limit translates to a maximum stub length of about 1 in.

If the slew rate can be slowed down, the stub length can be increased. But a slower slew rate can cause transition times that take up too much of the bit width and reduce the sample window.

Besides the transitions and receiver sample window, the bit width must allow time for skew. Consequently, the board designer must make a skew budget. Skew is caused by transceiver delay and varying stub and bus lengths. In a well-designed system, the skew for stubs, which range from 10 to 25 mm long, can be 100 ps. A typical bus with 10 loads spaced at 38 mm will have a maximum skew of 50 ps from line to line. A realistic driver and receiver prop delay and duty cycle skew would be about 600 ps. The total of 750 ps cuts down the 5-ns bit width to 4.25 ns available to capture data.



4. DERIVING THE RECEIVER reference voltage through a voltage divider from the termination voltage ensures that the noise margin high will remain constant.

By measuring the bit width from the 50% level for both high and low transitions, the designer can subtract half of the high-to-low transition and half of the low-to-high transition from the remaining bit-width allocation. A 1-ns transition time (10% to 90%) for each edge, which matches the desired slew rate of 0.8 V/ns for the 1-V swing, would then leave a 3.25-ns sample window time. This is enough for a high-performance differential receiver.

Noise margin in an LVS CMOS system is directly related to termination- and reference-voltage (V_{tt} and V_{REF}) stability. Using an appropriate circuit, noise margin high will remain constant because the receiver reference voltage is derived through a voltage divider from the termination voltage *(Fig. 4)*. So as V_{tt} varies, V_{REF} will track that variation.

But V_{ol} is independent of V_{tt}. Therefore, the low noise margin compresses as V_{tt} and V_{REF} track to a lower voltage. Because V_{ol} is also directly related to ground, noise margin low can be maintained by minimizing ground bounce for the driving transistors. Ground bounce is related to the inductance in the path to the ground plane and the sink current:

$$V_{gb} = L(di/dt)$$

Consequently, the sink current of up to 40 mA per channel must have a low-inductance path to the ground plane. One solution would be to add more ground pins.□

Stephen Kempainen, an application engineering manager in National Semiconductor's Advanced Systems Interface Products Group, received a BSEE from San Francisco State University.

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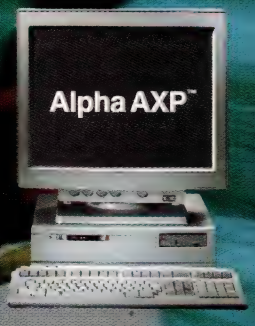

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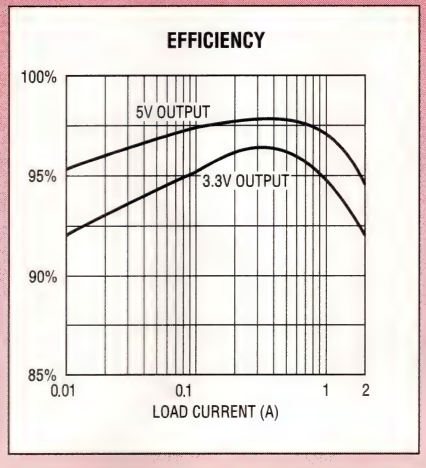
Both devices feature advanced Burst Mode™ power management circuity providing high efficiencies at load currents from a few milliamps to amps. Standby current is a low 160µA per regulator.

Both the LTC1142 and LTC1143 incorporate two independent regulator blocks providing 3.3V and 5V outputs with individual shutdown to less than 20µA. The LTC1142 operates over a 5V to 20V input range, allowing 10-12 cell battery packs.



The LTC1142 also supports full synchronous MOSFET switching for both regulator sections for efficiencies which can exceed 95%. The LTC1143 uses the fewest external components in the least amount of board space with efficiencies around 90%.

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CIRCLE 521

INDUCTOR-LESS LED BOOSTER

ALEXANDER L. BELOUSOV
Science Instruments Co., 6122 Reistertown Rd., Baltimore, MD 21215; (410) 764-2438.

In battery-powered devices with low operating voltage, a problem may arise in driving LEDs having more than 1.5 V of forward-bias voltage. This simple solution offers a way to drive the LED from one battery cell *(Fig. 1)*.

The circuit is based on a MAX660 charge-pump voltage inverter (the MAX665 could also be used). It employs a single carbon resistor and, instead of oxide capacitors, only a pair of inexpensive ceramic capacitors are used.

The current flowing through the LED is adjusted by varying resistor R_1 or capacitor C_1 *(see the table)*. Maximum current is about 25 mA with R_1 at 5.1 Ω.

A resistor of less than 5.1 Ω could also be used, but circuit efficiency will degrade and the battery-voltage ripple will increase.

The voltage on the LED is rather stable versus input voltage—it varies within about 10 mV when the battery voltage changes from 1.3 V to 3 V. Voltage ripple on the LED is less than 5 mV with resistor R_1 = 22 Ω. (Note that the circuit can be used as a low-voltage step-up voltage regulator in extra-low-voltage battery-powered devices when V_{CC} = 2 V or less).

Output voltage depends on the forward-bias voltage of the particular LED and may be within 1.5-2.0 V. In this instance, an LED featuring a forward-bias voltage of approximately 1.7 V was employed (therefore, the output-stabilized voltage was also 1.7 V). The circuit is able to handle a continuous output short if resistor R_1 should happen to be larger than 10 Ω.

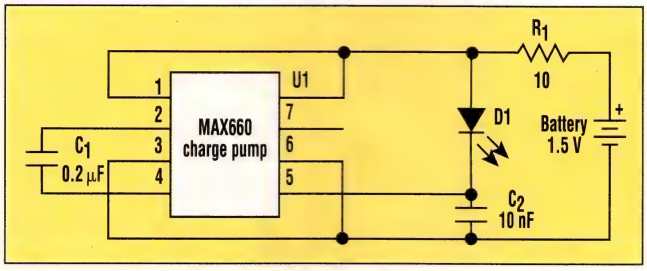
The positive battery terminal can act as a common power ground if current-limiting resistor R_1 is connected in series with the negative battery terminal instead of the positive terminal.

If needed, the circuit can be used as an economic flasher by applying short periodic pulses whose amplitude ranges from +1 V to $+V_{BAT}$ to pin 7 of the IC through the small-signal diode D1 (a low forward-bias voltage Schottky diode is preferable) *(Fig. 2)*.

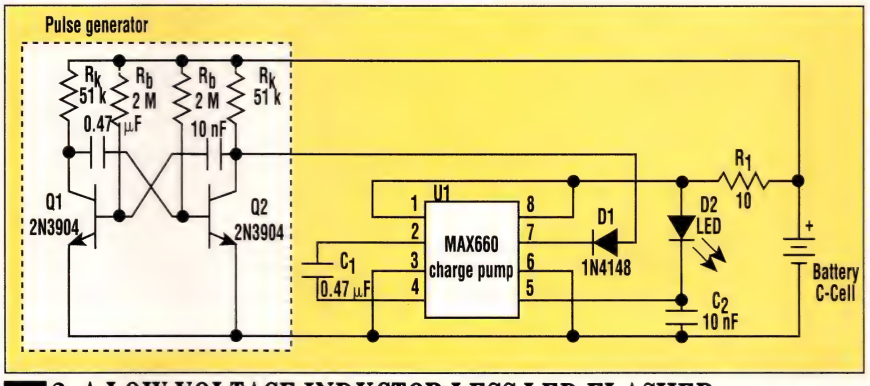
The circuit's average current consumption from the battery will be less than 0.3 mA. □

LED CURRENT VS. R1 AND C1

C_1 = 0.22 μF	R_1, Ω	22	10	5.1
	I_{LED}, mA	8.0	10	15
C_1 = 0.47 μF	R_1, Ω	22	10	5.1
	I_{LED}, mA	8.5	13	23



1. DRIVING an LED with more than 1.5 V of forward-bias voltage can be done with this simple inductor-less LED booster. The LED is driven from one battery cell.



2. A LOW-VOLTAGE INDUCTOR-LESS LED FLASHER can also be created from the circuit configuration of Figure 1. Outlined in the dashed box is a standard two-transistor multivibrator.

CIRCLE 522

GENERATING NESTED PULSES

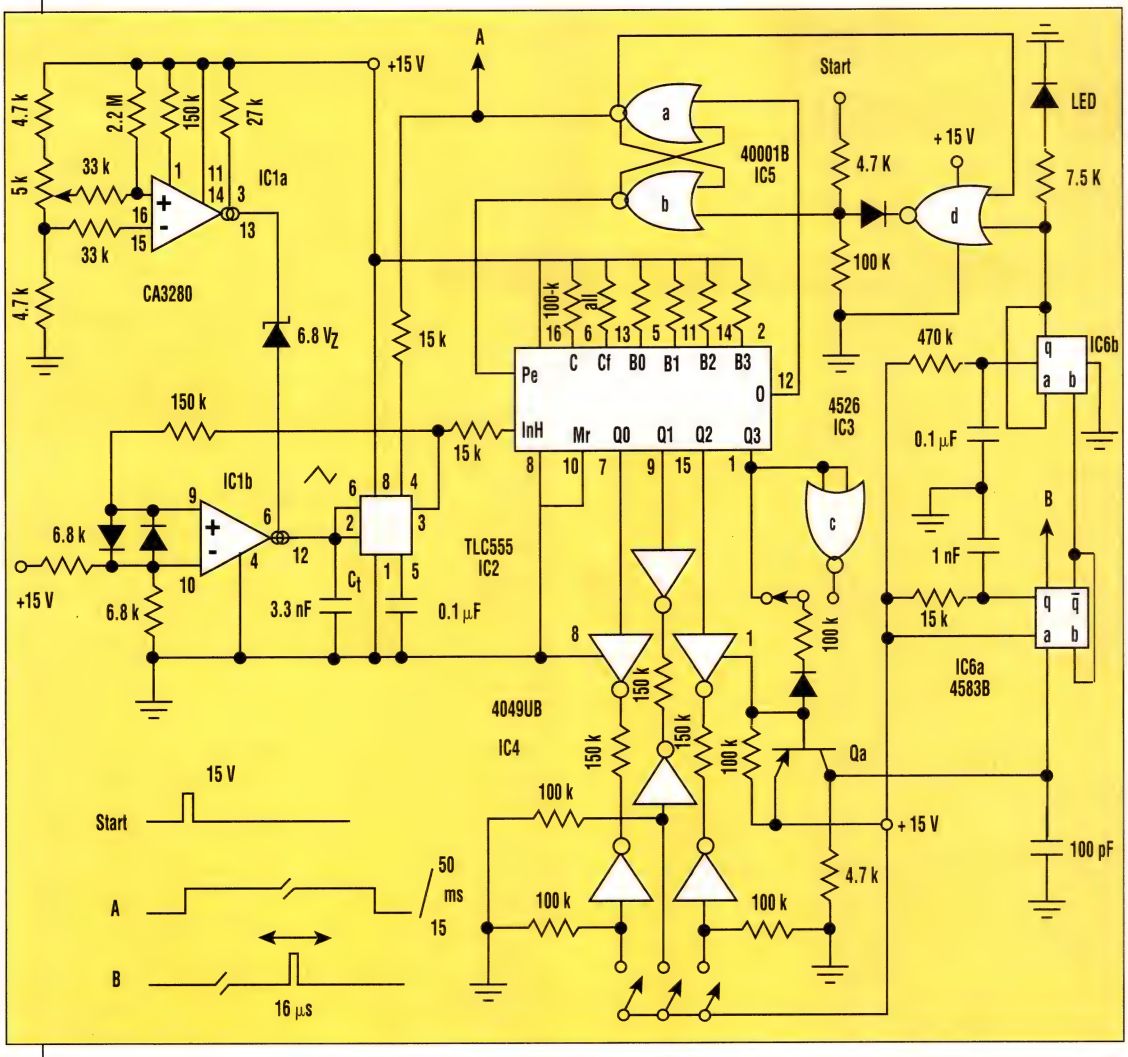
JOHN A. HAASE
Colorado State University, Fort Collins, CO 80523; (303) 491-5545.

This circuit layout offers an analog/digital technique for coordinated pulse generation *(see the figure)*. Pulse-width control is continuous while the dependent nested "B" pulse retains a discretely-selected time relation.

In the setup, pulse B occupies 1 of 15 time slots within the envelope of pulse A. This relation is independent of A's duration as set by the VCO (IC1b/IC2). Thus, one control will suffice for both a width and a delay setting.

The sequence begins when a Start pulse sets the R/S flip-flop (IC5a and IC5b) and releases the oscillator gate at pin 4.

Half of the dual OTA can now source or sink current into C_t when switched at lower and upper comparator thresholds of the 555 (IC2).



PULSE generation is coordinated in this nested pulse generator using an analog/digital technique. Width control is continuous; the "B" pulse retains a discretely selected time relation.

The other half serves as a voltage-controlled current source to pin 6, affording wide-range period adjustment for the triangle waveshape. The IC2 output from pin 3 is a square wave of the same frequency, which is able to drive the 4-bit down counter (IC3) at each negative transition. The initial count is 15, with decrements occurring once per oscillator cycle until the zero state at pin 12 terminates the cycle.

Pulse B is generated by comparing four bit switches with the counter state. Equivalence between the three lower-order bits implies that there is no voltage differential across the 150-k load resistors and no IC4 supply current. Consequently, transistor Qa is turned off.

Switch four at the MSB counter inhibits either the first- or second-half range by sinking base current through the diode. Collector voltage from transistor Qa triggers IC6a to produce the B pulse and IC6b in cascade as an optional LED drive to monitor the system's operation. When the circuit was tested, maximum recurrence rate was only 10 Hz for the Start pulse.

Alias retriggers are inhibited by the clamp gate at IC5d. Each sequence must run to completion before another Start pulse can be accepted. Note that a single-ended, +15-V power supply is employed for both the analog and the digital functions.

The OTAs are biased at mid voltage, and the comparator levels are fully compatible at one-third and two-thirds of V_s. As designed, the "A" pulse interfaces to an n-channel MOSFET (IRFD113) for power gain (as a solenoid drive), while the B pulse functions as an external trigger to a laser.□

IFD WINNER

IFD Winner for November 11, 1993

Biagio Presti, Aptron Laboratories Inc., P.O. Box 323, Bloomington, IN 47402; (812) 336-4775. His idea: *"Simplify Sync Stretch Circuit."*

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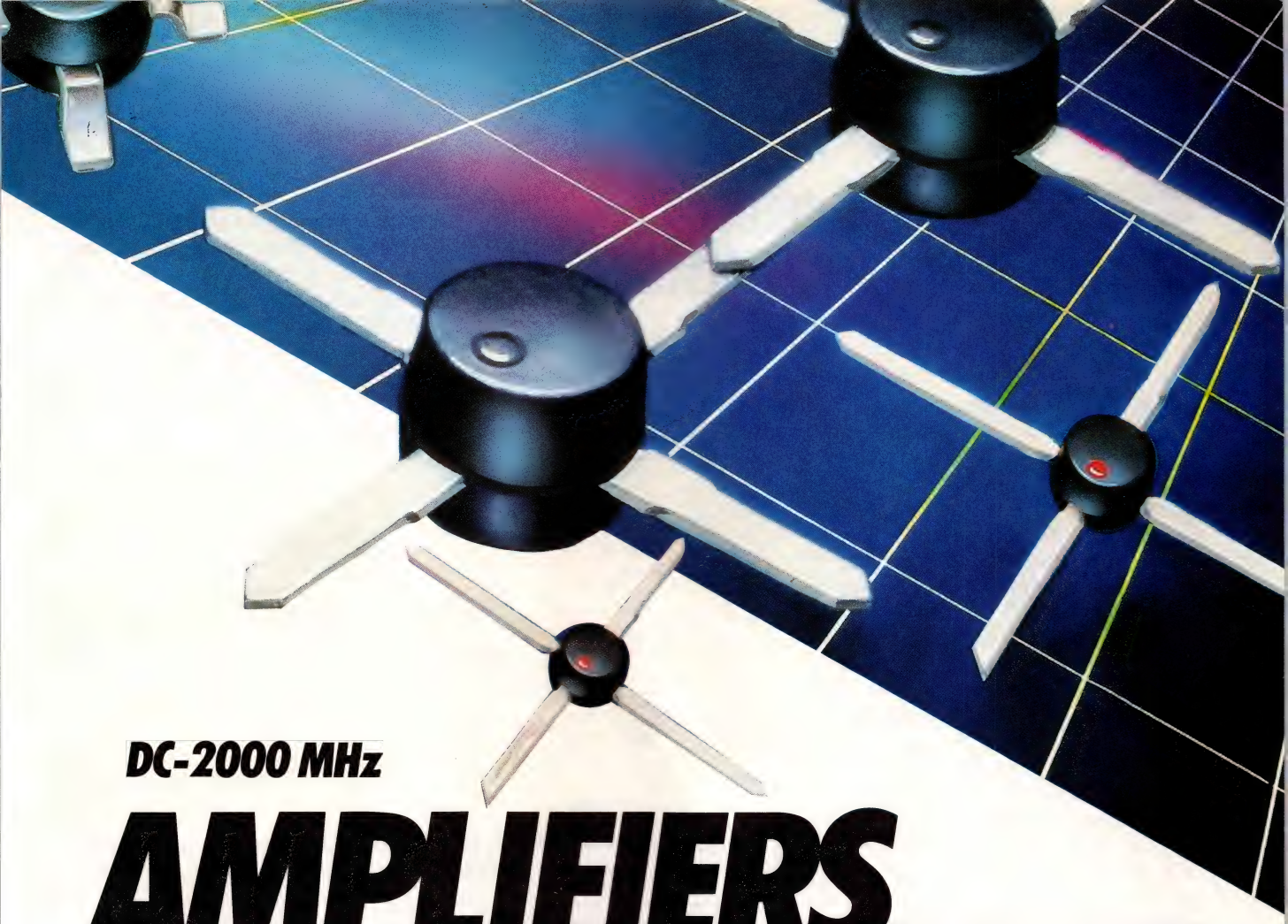

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Freq.MHz,DC to	1000	2000	2000	1000	2000	2000	1000	1000
Gain, dB at 100MHz	18.5	12.5	12.5	8.3	20	13.5	32.5	12.7
Output Pwr. +dBm	1.5	4.5	10.0	12.5	2.0	5.5	12.5	17.5
NF, dB	5.5	6.5	6.0	6.5	3.0	5.0	3.3	3.6

Notes: + Frequency range DC-1500MHz ++ Gain 1/2 dB less than shown

designer's amplifier kits

DAK-2: 5 of each MAR-model (35 pcs), only $59.95

DAK-2SM: 5 of each MAR-SM model (35 pcs) only $61.95

DAK-3: 3 of each MAR, MAR-SM, MAV-11, MAV-11SM (48 pcs) $74.95

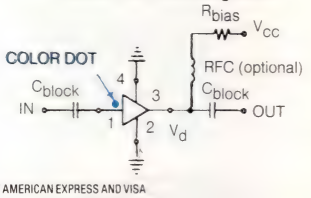
designer's chip capacitor kit

KCAP-1: 50 of 17 values, 10pf to 0.1μf (850 pc), $99.95

chip coupling capacitors at .12¢ each (50 min.)

Size (mils)	Value
80 x 50	10, 22, 47, 68, 100, 220, 470, 680 pf
80 x 50	1000, 2200, 4700, 6800, 10,000 pf
120 x 60	.022, .047, .068, .1μf

Typical Circuit Arrangement



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For detailed specs on all Mini-Circuits products refer to • THOMAS REGISTER Vol. 23 • MICROWAVES PRODUCT DIRECTORY • EEM • MINI-CIRCUITS' 740-pg HANDBOOK.

F154 REV. A

READER SERVICE 104

CIRCLE 523

BUILD EFFICIENT DC LAMP DIMMER

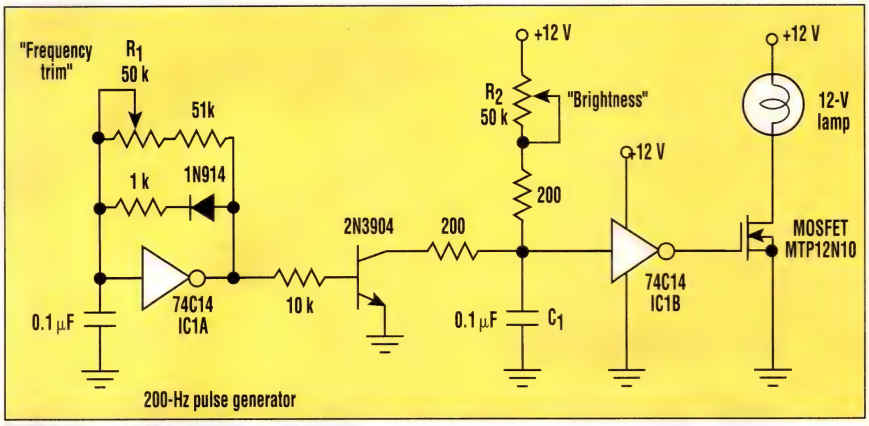
DAN RETZINGER
17113 Baltar St., Van Nuys, CA 91406.

Often, a linear-regulator scheme is employed to control dc lamp brightness. However, this "brute force" approach usually is worse than 50% efficient. An alternative is the pulse-width-modulated approach, which can yield an efficiency of 96% or better *(see the figure)*.

Inverter IC1A forms a narrow pulse oscillator with a frequency of about 200 Hz, and a pulse width of approximately 0.1 ms. Potentiometer R_1 sets the oscillator's frequency as well as the end limit of R_2, which is the brightness control. The charge time on C_1, set by adjusting R_2, varies the pulse width from narrow to wide.

R_2 provides a good linear brightness adjustment that includes the extremes of fully off to 100% on. With lamp loads of up to 24 W, the there's no need for a heat sink on the power MOSFET. The circuit's inefficiency is due mainly to the voltage drop across the MOSFET (using a power MOSFET with a lower RDS-on produces a more efficient circuit).

The circuit is suitable for controlling heating elements as well as some dc motors.□



THIS DC LAMP DIMMER, which uses a pulse-width-modulated approach in place of the typical linear-regulator scheme, has an efficiency of 96% or better.

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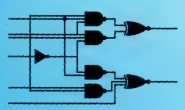

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EDITORIAL CALL WANTED: SOFTWARE IDEAS FOR DESIGN

Electronic Design will publish five special supplements during 1994 focused on engineering software. For those supplements, we are looking for the software equivalents to Ideas for Design: brief, tightly focused articles that describe short software routines, problem-solving tips on writing embedded code, etc.

We will pay $100 for each Engineering Software IFD we publish. Articles should be a maximum of approximately one typewritten page of text with one or two code listings or block diagrams. They should represent the author's original work, and should not have been previously published.

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A 32-macrocell EPLD for the cost of a 22V10? Bob found this to be a rather pleasant surprise.

If you're currently designing with 22V10s or other PALs or GALs, then you're ready for the advantages of Altera's EPM7032. Here's a device that triples the density of what you're currently using; saving board space and decreasing power consumption. With pin-to-pin delays as fast as 7.5 ns, you'll be able to support even the fastest Pentium designs. But the real value is that you get these powerful, high-performance features for less than the cost of a 22V10.

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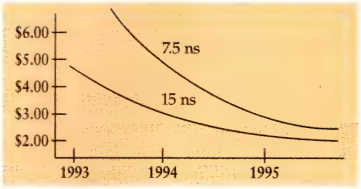
Tpd = 10.0 ns	$ 7.95	$ 9.90
Tpd = 7.5 ns	$11.95	$14.25

Above prices are based on 100 piece quantities. Pricing for the 22V10 is based on the lowest of the published prices from Lattice and AMD as of January 1, 1994.



EPM7032 projected 25,000 unit pricing through 1995.

The ALTERA Advantage

Altera Corporation, 2610 Orchard Parkway, San Jose, CA 95134-2020

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READER SERVICE 136

graphical programming languages *have certain limitations when it comes to test development. •No one has figured out a way to let you create tests as powerful as the ones you're running now. •No one has figured out how to control every instrument you're likely to use. •No one has figured out a way to let you leverage your existing code. •If anyone ever figures this stuff out,* there's going to be a big noise about it.

Ba

HP VEE: Here's one graphical programming language you'll like the sound of.

Test programming. There's no getting around it. So you plod your way through it using a tedious text-based language. Or, you try a graphical programming language that may force you into compromises you're not prepared to make.

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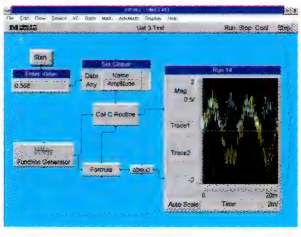
The only graphical programming language designed specifically for test engineering, HP VEE cuts test development time by allowing you to literally "flowchart" your way through a test program with remarkable speed. And, more importantly, without compromise.



Standard language ties give you the flexibility to use existing code or create new C routines.

Hundreds of full-featured drivers and Direct I/O allow you to control every instrument.

Now there's no limit to the power of your test programs.

Every aspect of HP VEE reflects a profound understanding of the test environment. Instrument control is complete, robust and logical with a built-in test sequencer that provides the framework for test development.

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With HP VEE, data can be taken from instruments, generated internally or accessed from existing files. And, it can be manipulated with anything from simple addition

ng!

to your custom formulas, then presented in the form you want.

There's no limit to the instruments you can support.

If you have it, HP VEE supports it. The choice of instrument control is yours. In addition to more than 350 full-featured drivers that come standard with the software, HP VEE's Direct I/O lets you send any command to any instrument. If you need custom drivers, a built-in driver writer makes it easy to create custom drivers in minutes.

There's no limit to how much you can leverage your existing programs.

HP VEE frees you from proprietary solutions. There is no need to rewrite your code or routines. Standard language ties allow you to import and use what you already have in place — including C, C++, HP BASIC, FORTRAN and Pascal. Or, you can write new routines in these languages and use HP VEE's DLL ties.

An utterly open system, HP VEE runs on Windows-based PCs, Sun and HP-UX workstations. And, it supports multiple I/O interfaces from various vendors — reflecting the reality of test engineering.

Discover what all the noise is about. Call for your free preview disk today.

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ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Mobile computing has arrived—computers are proliferating in industrial settings and portable computing devices in all sizes have become the liveliest performers in the PC market. Alternatives to keyboard input have become more important. After some false starts, pen input, touch screens, and voice input now show good potential for growth. Compound annual revenue growth should amount to 44% for pen devices; 25.6% for voice input; and 16.5% for touch screens. These predictions are drawn from Venture Development Corp.'s report, *The U.S. Market for Keyboard Alternative Input Devices.*

Because prices are dropping sharply, unit shipments of all types of input devices (including trackballs, mice, and digitizing tablets) will increase faster than revenues, according to the Natick, Mass.-based market research company. Total unit shipments should increase at a compound annual rate of 16% while revenues are expected to increase only 10.9%.

There will be a shift away from light pens, used with CRTs, toward pen digitizers for LCDs; smaller digitizers are coming to the fore, owing to the growing popularity of handheld machines in place of larger tablets and notebook computers. Unit shipments, Venture Development predicts, should increase at a 79% annual rate.

KEYBOARD ALTERNATIVES POISED FOR STRONG GROWTH
(millions of dollars)

	1994	1995	1996	1997
Pointing devices	414.6	441.4	464.3	484.4
Pen input	28.9	41.6	59.4	84.3
Touch screens	150.1	168.8	184.4	198.8
Graphics tablets	160.8	168.0	175.9	184.5
Voice input	61.3	76.9	97.3	124.1
Total	815.7	896.7	981.3	1076.1

Source: Venture Development Corp.

QUICK REVIEWS

Ace the Technical Interview: How to Get Your Next Job in the Computer Industry gives answers to 2000 technical questions likely to be asked by job interviewers. Written by Michael Rothstein, formerly a systems engineer for IBM Corp., the book examines the job search process and describes interview scenarios. Rothstein maintains that a job applicant can learn to spot trick questions in interviews and learn to respond successfully to them. The book discusses a range of computer technology, emphasizing the knowledge needed in today's difficult and changing job market. Each technical chapter contains 70 to 100 questions to test readers' knowledge of the material. (McGraw-Hill, 420 pages, paperback, $19.95; ISBN 0-07-054030-6) (800) 262-4729; (212) 337-5951.

Code Complete: A Practical Handbook of Software Construction, written by Steve McConnell, is a reference book intended to improve the programming practices of a broad audience of students, self-taught programmers, technical managers, as well as experienced developers. Readers who know a procedural language should be able to follow the book's examples in C, Pascal, Basic, Ada, and Fortran. McConnell has collected practical ideas and methods for implementing software from universities, software engineering laboratories, and commercial environments at Aldus, Boeing, IBM, Microsoft, TRW, and others. These methods, which are aimed at helping developers create higher quality software and increase productivity, could save years of having to learn by doing. *Code Complete* is $35 from Microsoft Press, P. O. Box 7005, La Vergne, TN 37086-9954; (800) 677-7377.

The Little PC Book belies its title in the amount of basic information about IBM PCs and compatibles packed into 376 pages. The book answers common questions such as "Is it safe to buy through mail order?"and is written by Lawrence Magid, founder of a PC training company, and online columnist and computer book author. The book also includes The DOS Cookbook, step-by-step instructions for 63 everyday DOS tasks as well as The Windows Cookbook, which gives step by step instructions for 71 everyday Windows tasks.

Because of the cookbooks, the book is useful even to experienced PC users, who may never have cracked a DOS manual or Windows documentation. The eye-catching illustrations by John Grimes show how peripherals are connected and illuminate other computing concepts. The book, published by Peachpit Press, has a list price of $17.95. The address for Peachpit Press is 2414 Sixth St., Berkeley, CA 94710; (800) 283-9444; (510) 548-4393; fax -5991.

The High-Tech Joke Book is a compilation of jokes, puns, riddles, definitions, and anecdotes from the engineering, scientific, and computer communities. As the book jacket points out, those who think there is no humor in high technology shouldn't bother to read the book. For example, how many hardware engineers does it take to change a lightbulb? None. "We'll fix it in software." In another example, how many software engineers does it take to change a lightbulb? None. "We'll document it in the manual." The book is $14.95, plus $1.50 for postage and handling, from Oak Ridge Public Relations Inc., 21771 Stevens Creek Blvd., Suite 203, Cupertino, CA 95014-1175.

QUICKLOOK

OFFERS YOU CAN'T REFUSE

A video demonstrates Megatek's Maxim X-Cellerator, a VME graphics coprocessor board with X-Cellerator Windows software. Maxim is supported by Data General, Encore, Force, Harris, Hewlett-Packard, Motorola, Radstone, Sun Microsystems, Themis, and other VME-based computers. For a free copy of the video, contact Megatek Corp., 9645 Scranton Rd., San Diego, CA (619) 455-5590; fax 453-7603. CIRCLE 460

A directory of sources and suppliers for MIL-STD-1553 components is available on the SAE Avionic Systems Division Electronic Bulletin Board System. To access the BBS, login with your computer and modem to (800) 733-7837. At the main menu select <C>ommittee, then <1>AS-1..., then select <D>ownload. Contact Rich Vandame or Barb Roth on the BBS or at the Society of Automotive Engineers, 400 Commonwealth Dr., Warrendale, PA 15096-001; (412) 776-4841, ext. 292; fax -5760. CIRCLE 461

Computer users are becoming more adept at gleaning information from databases; unfortunately, graphics data in the form of charts and illustrations often remains illegible. As a result, NIST (National Institute of Standards and Technology) researchers are looking for industrial and academic partners to join a cooperative research consortium to develop technology for virtual libraries. These would enable desktop computer users to access documents on a computer network and view them as they appear in published form. Adobe Systems Inc. has already signed on to the R&D effort. For more information, contact Lawrence A. Welsch, B254 Technology Bldg., NIST, Gaithersburg, MD 20899-0001; (301) 975-3345; fax 926-3696; e-mail welsch@ncsl.nist.gov (via Internet).

A free two-hour seminar covers SuperScope II instrumentation software for the Mac. The program monitors and controls IEEE-488 and RS-232 devices, reads analog outputs (d-a) and performs digital I/O through GW Instrument's MacADIOS data-acquisition hardware. SuperScope can export data to spreadsheets, word processors, databases, and graphing and math programs. Reservations are required; contact GW Instruments, 35 Medford St., Somerville, MA 02143-4237; (617) 625-4096; fax -1322. CIRCLE 462

QUICK NEWS: • CONFERENCES

Courses on fuzzy logic (4532) and understanding and applying artificial neural networks (4531) will be held March 28-29 and March 30-April 1, 1994 at the University of Wisconsin—Madison. Included are notes, a textbook, and for neural networks, a free software demonstration package. Participants in both courses receive a 10% fee discount. For information, contact UW, Engineering Professional Development, 432 N. Lake St., Madison, WI 53706; (800) 462-0876 or (608) 262-2068; fax (608) 263-3160.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (408) 446-4458; fax (408) 253-6085

I've been working on a paper entitled, "How Am I Doing on Time-focused New Product Development?" for this year's Portable by Design conference and exhibition. I understand the title of the paper only too well. For me, it's a business that I've been working with for an extended period of time helping new product developers get product out in a timely fashion. Often my financial compensation is directly linked to the timeliness of the product's introduction and its future financial good fortune. So when someone comes up and asks "How am I doing on time-focused new product development?" I need an accurate answer for a number of reasons. To provide the answer, I look at five areas of organization performance and search for a response to the following questions:

1. Does the product development organization, from executive manager through team member, know what time is worth?
2. Are products defined as a continuum to produce a sequence of product introductions through time?
3. Is a documented new product development process, based on "speed profile" principles, in place and is it being effectively utilized?
4. Does the organization effectively apply the equation:

   Work quantity/commitment = duration?
5. Is each new product effort managed in real-time using a database?

Knowing the right questions to ask leads to the identification of where potential performance problems reside. If the value of time is not known, how can appropriate trade-offs between development time and its interaction with the lifetime profitability of the new product be made? Working toward one big goal that covers all bases could produce a winning new product, but what if its definition misses a few things and it turns out to be a business flop?

ince new product development is a team effort, is it really possible to work effectively without a process to follow that is understood by all team members on a cross-functional basis? Work is real and any undertaking contains so many hours of it, so how is it divided up between a finite number of resources to get the job done on time? And no effort runs independently of other work taking place within the same product development environment, so how are trade-offs between competing internal demands appropriately dealt with? A new product development organization that quickly, consistently, and correctly gets to the answers on these questions wins the time to market challenge.

Regular readers of the column should have some of the answers to questions 1 through 4. Each of these topics has been addressed over the past three years in relative detail, although on the installment plan. Question 5 has received minimal treatment in the column to date. I'll be putting effort into new product databases over the next few months.

More information on this topic is contained in New Product Development: Design and Analysis, which can be obtained by calling Time to Market Associates.

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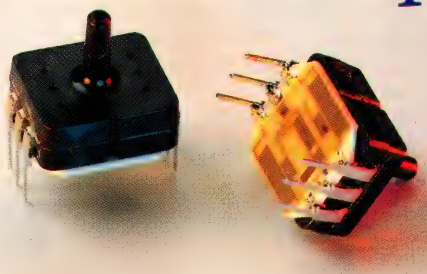
Then try our new . . . chips 'n dip



This combination should prove to be very appetizing, even to the most discriminating taste — especially when it comes to selecting the best combination of quality performance, attractive pricing and ease of assembly.

SenSym's new **SDX** Series offers temperature compensated sensors from **1 psi to 100 psi** in a small, low cost, machine insertable, rugged, plastic package.

So — with our **SDX** Series you can work less, worry less and just kick back and enjoy the party. The first **sample is free.**

If you want a "taste", just call **(800) 45-SENSYM**, or complete and return the form below.

In the **100 piece** party pack, the **SDX** is only **$13.90** each. Why not stock up for the special occasions?

Compare the label on our SDX Chips and DIP with competitive brands (*Typical Specs*):

• Full-Scale Span	up to 100mV	• Temp. Effect on Span	±0.4% FSO
• Span Calibration	±3.5% FSO	• Temp. Effect on Offset	±0.2mV
• Compensated Range	0°C to +50°C	• Long Term Stability	±0.1% FSO
• Operating Range	–40°C to +85°C	• Response Time	100 µsec
• Linearity & Hysteresis	±0.2% FSO	• Input/Output Z	4K
• Zero Pressure Offset	0 ± 1mV		

ED

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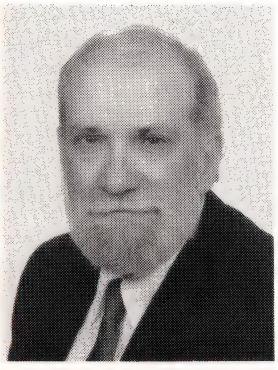
MY VIEW

...The promise chain

BY FRANK J. BURGE
Director of Market Development
for Electronic Design



Much was made about the sign in Bill Clinton's campaign headquarters: "It's the economy, stupid." Clinton's focus on the economy became his ticket to the White House. In the electronics game, the sign in the CEO's office might well read: "It's time to market, stupid." Read the market right, get your PC there first, and you'll have the advantage. This is true in wireless, workstations, software, and everything else.

Every OEM manufacturer's TTM strategy depends on its suppliers. OEMs are particularly dependent on the semiconductor industry since it provides the breakthrough technologies that enable end-market creation and growth. Often these breakthrough products are sole source/only source—dependence squared. But the OEM's time-to-market expectations involve more that just getting those hot new semiconductor parts on time and with the expected quality.

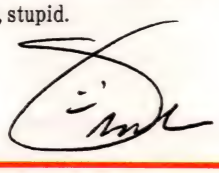
Other softer issues affect the relationship. One is trusting that the supplier will be responsive to your needs, promise what it can deliver, and deliver what it promises. Your ability to get your new product to market depends on getting speedy response to your questions. Some suppliers do a terrific job of getting answers and keeping promises. Others don't do so well.

Why is that? Well, my barber figures it relates to what he calls "the promise chain." Major suppliers have invested megabucks in information technology so they can answer your telephone inquiries, so they can be responsive. The mission may be to answer 95% of all customer inquiries on the spot and answer the remaining 5% within one hour. My guess is such service would delight most OEM customers. And delighting customers creates a competitive advantage.

Now with all these bucks invested in the latest information systems, why are some companies so much better than others at giving you answers? The promise chain again.

Let's assume that I work in customer service. You call me and ask for simple price and delivery information on several parts, including a hot new IC to be used in a new system design. I give you the answers you want except that information on the hot new gizmo isn't in my information system. So I can't satisfy your request.

Well why isn't the information in the system? Probably because some guy in product marketing or production control refused to input it into the system. Because he or she wanted to have control, the power that comes with having information and deciding which business is accepted at what price. So what do I do? Since I can't give you the information you need, I promise to get it for you. Keep in mind my mission is to get you the answer in one hour. So I call my product marketing person. What is a typical response? "I can give you a bad answer now or a good answer tomorrow." Meanwhile you, the customer, are twisting in the wind waiting for an answer. And I have failed to deliver on my one-hour commitment because the product marketing person doesn't have ownership in the one-hour response initiative. Timely response to customer requests isn't in his job description. People make promises to customers based on what someone else tells them. And that someone else probably gets input from someone else and so on. In every company a promise chain runs up and down and across the organization. And the ultimate promise to the customer is only as good as the weakest link in that chain. Yet I'm continually amazed at how many well-meaning companies consistently disappoint customers by being nonresponsive to requests and by breaking promises, never understanding why. It's the promise chain, stupid.



Everybody's Talking About
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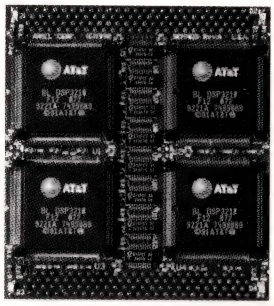

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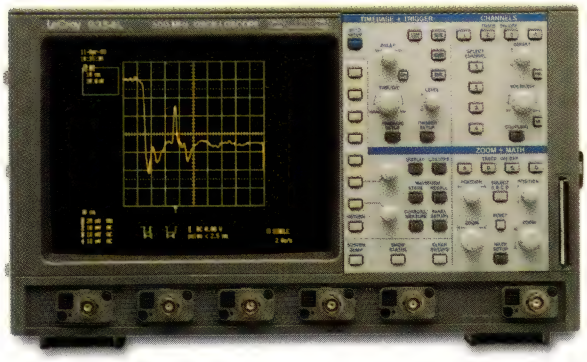

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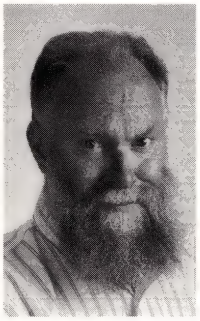
WHAT'S ALL THIS TECHNICAL READING STUFF, ANYHOW?

Recently a young engineer, Barrett L. of Poughkeepsie N.Y., wrote me a letter. He not only ordered one of my books, but he asked my advice and opinion: "I'm a recent E.E. graduate, and if you could please supply me with a list of suggested reading (i.e. books, periodicals, columns) it would be greatly appreciated." Well, I *had* to reply:

"Dear Mr. L.—Darn it, you are the second person this week to ask me this question, and while I was stupid enough not to get the message the first time, I won't miss the message twice. Fortunately, there are several good books I can recommend.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

You have not gone wrong in ordering my book on *Troubleshooting Analog Circuits*.[1] I try to keep things light and breezy, with REAL examples. And I also try to minimize the platitudes, as you have noted that nothing gets me TICKED OFF faster than meaningless platitudes. I think real engineers get their education from EXAMPLES, and I try to write accordingly.

A second related book, from the same publishers, is *Analog Circuit Design*[2], edited by Jim Williams. It consists of about 33 chapters from 23 authors. It, too, is educational in terms of EXAMPLES. Some of the chapters are so-so (in my opinion) and then they get better and better, up to *great*. The chapters by John Addis and Derek Bowers are great. I wrote two good chapters.

NOW, if you laid hands on this book you might decide that you wanted to buy it, OR you might read a few chapters and then put it back on the shelf. So get your librarian—your town librarian or your company librarian—to order it. If you ain't on good terms with your librarian, you *should be*. After the librarian buys it, it can be shared by a good number of people.

Nextly, there's Horowitz and Hill's *The Art of Electronics*.[3] Any bookstore will order it for you. It's in its second edition—very popular, fun to read, good insights. Your company librarian would be wise to buy this one if there are more than six engineers in your company. Maybe you have read this already. It's a good reference book. If there are older engineers who went through school before this book came out, or technicians, they may find this of high value.

At this point, I gotta ask you, Barrett, where are you *coming from*? What good electronics books have you read? Did you take a lot of electronics courses? How many analog, how many digital, how many software? I can assure you, I can give you ZERO advice on software. I have written a couple of successful chunks of BASIC, but my opinions are worthless. I can't give you much advice on digital circuits, and books thereon, but I'll ask my friends.

Next question for you—in which direction do you think you are *going*?? Analog, ADCs, or systems? Low power? High speed? Lotsa processors and a little analog? Just trying to get a broader education? That will make some difference. Or, if you're not sure where you're headed, well, the broad perception from reading a lot will be good for you.

OF COURSE you gotta keep reading *Electronic Design*.[4] It gives you a good clear presentation of some of the newer ideas, circuits, concepts, and trends, with intelligent guys from the industry trying to make good explanations—trying to play teacher. One item of advice: Read and mark the hell out of any stories that are interesting. Xerox or cross-index the stories that are of good interest, but don't throw the magazines away for at least five years. You can go back in several years and see what's interesting, what's trivial, and what's passé. Note, a five-year stack of ED just fills two "Xerox-paper boxes," about 2.5 cubic feet....

Read hobby magazines —*Popular Electronics*[5] or similar publications. Some of the stuff is trivial, but that's OK—sometimes it's good to read stuff where you're smarter than the authors, and you can see if they're doing something stupid.

James Roberge of MIT wrote an excellent book about op amps in general, and about the LM301A in particular.[6] The first half explains how the '301 chip was engineered; the second half goes into how you can *apply* a '301. I asked James and he said it's still in print. It's a very good read.

The advanced, expert book on op amps is by Jiri Dostal—*Operational Amplifiers (second edition)*[7]. I'm selling these for $53. This used to sell for $113 from Elsevier Scientific, and was worth it. Now at $53, it's a bargain. Serious, thoughtful. NOT your FIRST primer on op amps, but any serious user of op amps should read this about once a year. You'll learn something new every time. However, that statement is true for almost every one of these books: All of these books are well worth rereading every year or two.

Now, darn near your first primer on op amps is Tom Frederiksen's *Intuitive IC Op Amps*.[8] Heck of a fine book. Where is it sold? Tom still has some to

sell. If you want to use op amps, you want to do it intuitively. No fancy formulae, no matrices, no Taguchi optimization. Just common-sense engineering with good intuitive insights. Tom's an excellent teacher for that.

The NEXT primer on op amps is NSC's linear databook on op amps.[9] The history of op amps was written there.

NOW, Analog Devices' op-amp databook might be almost as good as NSC's, *but* they usually don't include device schematics. If you want an AD databook, call them up.[10] You can request and study databooks from anybody in the whole electronics industry, but I find the ones that do include schematic diagrams (of the devices themselves) are the most useful and educational.

NEXT, NSC's *Linear Applications Handbook*.[11] Some of the better early linear IC applications breakthroughs have gone into there. It's indexed pretty well, so you can find what you want.

NSC's databook on regulators and power ICs[12] is quite good—a useful basic reference book. Also falling into that category is the *Data Acquisition Databook*[13], which covers DACs, ADCs, voltage references, and temperature sensors. Another is the *Linear Applications-Specific ICs Databook*,[14] which includes several strange but useful ICs.

The list price for these NSC handbooks is usually about $10 or $15 *each*. But our marketing guys agreed that we ought to make a special offer to readers of *Electronic Design*—serious engineers. If you want any or all five of those linear databooks, just call and ask for the set.[15] Not a bad deal.

If you ever have to do "optimization" or quality problem-solving, buy the books that cite "Taguchi" in them the *fewest* number of times. I just got around to reading Keki Bhote's book[16], full of excellent common sense. I started out skeptical, but eventually decided I really liked his style and common-sense approaches. Hans Bajaria has a good book.[17] So does Forrest Breyfogle.[18] And Diamond's book[19] is good, too. Just keep away from books by Genichi Taguchi, and all his friends who tell you how great it is to use orthogonal matrices to solve any problem and you don't have to think... (if you know what I mean, and I think you do).

Recently, I was introduced to a new book by Dennis Feucht, *Handbook of Analog Circuit Design*.[20] It really covers lots of the things a designer needs to know about analog circuits. I'm favorably impressed, and I recommend it. It has good chapters on wideband amplification, precision amplification, feedback circuits, frequency compensation, signal-processing circuits, etc. There's some overlap with Hill and Horowitz, but that's *good*, not bad.

Another good new book is *High-speed Digital Design*, by Howard Johnson, subtitled *A Handbook of Black Magic*.[21] I thought it was pretty good, so I loaned this to one of our best digital/mixed-signal designers. I was a little surprised when he returned it right away. He said that was because he had gone out and bought several copies for the guys in his group. It treats the gray area between signals that are digital, and the analog aspects that are so important when you want your digital buses to behave at higher and higher speeds—not a trivial task. This book is there to help, with serious advice and good philosophy. You ain't gonna get much of that anywhere else these days.

One of my old fans, Reg Neale, recommended a book on ESD, *ESD from A to Z*, by John Kolyer.[22] I discovered the book in our library, read through it, and found a number of thoughtful observations. Just as my book is the "best" book on Troubleshooting, so this book may well be the "best" on ESD, and *partly* for the same reason—it's the only one.

When I wrote about Ground Noise in June, I recommended the excellent book by John Barnes, *Electronic System Design*,[23] and I still do. Also, a friend recommended *Noise Reduction Techniques in Electronic Systems*, by Henry Ott.[24] Its second edition just came out, and it, too, covers many topics that aren't taught in schools. If you work with RFI and EMI in real systems, you'll probably profit by buying and reading *both* of these books.

Recently, Barrett, a reader asked me what book can I recommend to teach about designing printed-circuit boards? I asked several friends—no ideas, no recommendation. Maybe some of our readers can recommend a book? There *ought* to be something beyond the literature of the pc-board-design software people...

Also, you and other readers who recall the question and debate of the value of a Bachelor's Degree versus an Associate's Degree in Electronics Technology may be interested in a new book by Joel Butler, *High-Technology Degree Alternatives*.[25] He observes that you don't have to go to school at night for a dozen years, nor drop out of work and pay tuition for four years. He has several suggestions on how you can get credit for school courses and work you have already accomplished. He recommends a list of a few dozen schools where you can apply by mail. This sounds kind of unlikely, except Mr. Butler points out that these schools actually are ACCREDITED, which isn't a trivial statement.

One last "book," actually some stories on floppies, was sent to me by Geoff Harries, a reader located in Munich, Germany. They are Science Fiction, sort of high-tech and time-travel, and good historical stuff, too. He's still trying to get a publisher. Meanwhile he gave me permission to sell you his book, *ChronDisp I* (about 700 kbytes) on a high-density IBM-type floppy for about the same price as a paperback book. I will repatriate all proceeds to Geoff. I enjoyed the book, and I recommend it to you, too. It's kind of fun to sit there in the evening, hitting "Page Down," again and again, reading Geoff's stories.[26]

Well, there is my list. This may not be a DEFINITIVE list, but it's a good start. Ask your buddies. Borrow some of their hobby magazines. Also, you will probably want to read one or two general-purpose science magazines. I used to read *Scientific American*,[27] but a year ago I gave up on them and changed over to *Discover*.[28] Maybe *Sci Am* is coming back, but I still think *Discover* is excellent. Try *Machine Design*.[29] You can spend a lot of time reading this, but it's fun and educa-

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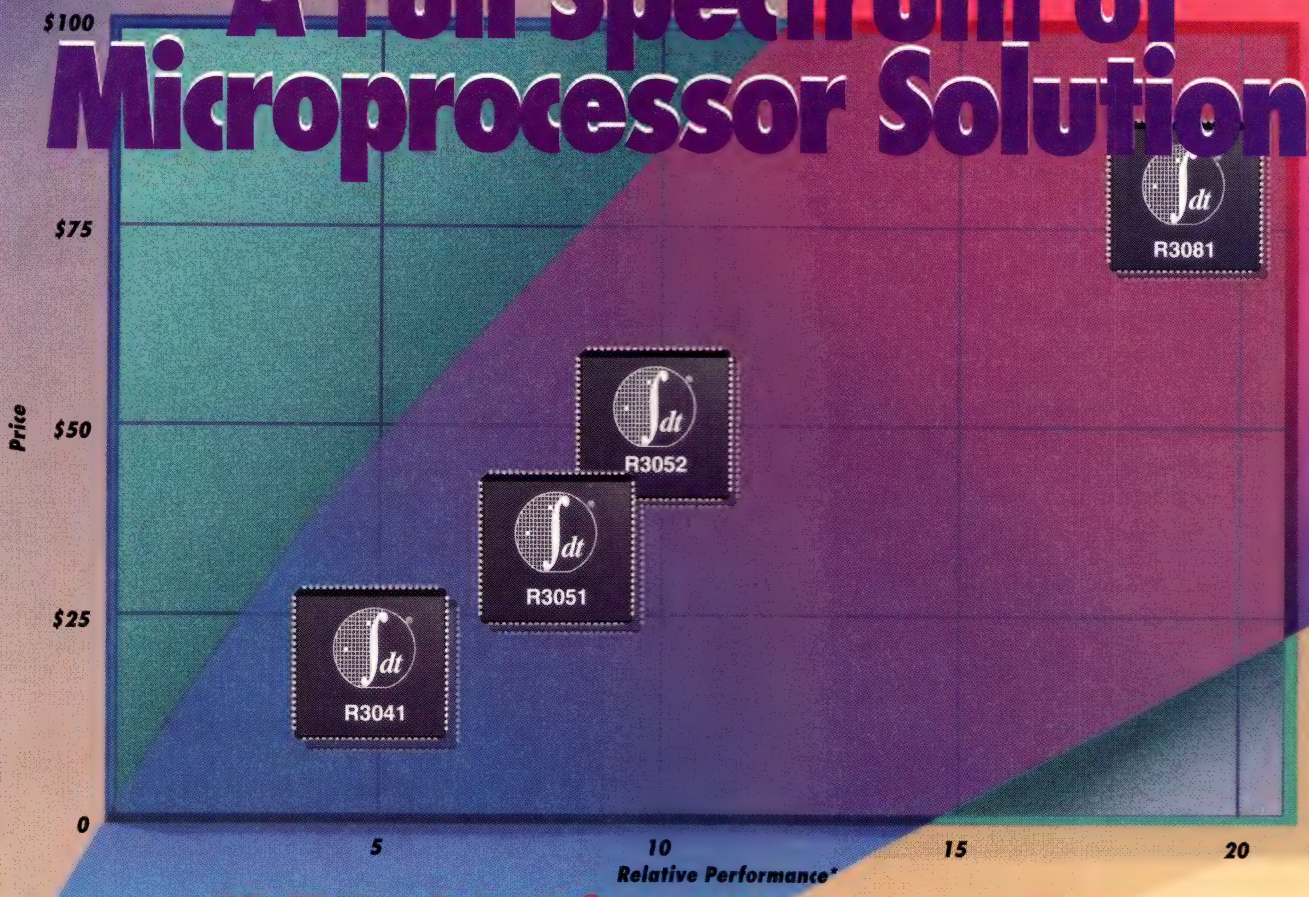

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tional. You'll see several kinds of good engineering.

Ah—yes, let's not overlook the obvious. You should also read *your own company's* catalog or data sheets. Look at what it says to your customers, and look at the circuits "behind the front panel." I don't know what your company does or makes, but let's assume there are PRODUCTS somewhere. When I joined Philbrick in '61, I studied the heck out of all its schematics and data sheets, op amps, and analog computing products. Then I would say to myself, "Why did they do *that*?" I surely couldn't understand everything, but by asking all questions that came to mind, I got a *heck* of an education.

Similarly, when I came to NSC in 1976, I studied all of the op amps, data sheets, schematics, AND layouts. I'm sure you will agree that in an IC, the layout can be even more important than the schematic. In my first year at NSC, I spotted a philosophical error in the layout of a popular amplifier. The changes I suggested caused the yield to go up on the LF356, the LF256, AND the LF156, by a factor of 2, EACH. That yield improvement paid for my first couple years' salary, even if I had done nothing else.... So, read your own company's literature, and the serious art (schematics, layout, software, or whatever) that's behind the scenes.

NOW you can plainly see that I have written a whole *column* around your request, for pity's sake! I hope I have answered the question for you *and* for many other guys who are just out of school and trying to get going—up the LEARNING CURVE. So, read books and think of good questions. When you have answered as many as you can, and you have asked your colleagues, and there are still some you cannot answer, write down some notes and ask one of your Senior Engineers. He'll probably be flattered to get thoughtful questions from a *serious* student. If you ask reasonably, he/she may provide some (priceless) mentoring. Have fun, Barrett!!"

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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1. *Troubleshooting Analog Circuits*, 3rd Printing, Robert A. Pease, 1992, 208 pages. Butterworth-Heinemann. Order from Robert Pease, 682 Miramar Ave., San Francisco, CA 94112. NOW in PAPERBACK—NEW LOW PRICE—$25.95 including tax & shipping.
2. *Analog Circuit Design: Art, Science, and Personalities*, edited by Jim Williams, 1992, 222 pages. Order from Robert Pease, (see address in reference 1) $47.95 includes tax & shipping; or order it from the publishers, Butterworth-Heinemann, Stoneham, MA; (800) 366-2665 or (617) 438-8464.
3. *The Art of Electronics* (2nd Edition), Paul Horowitz and Winfield Hill, 1989, 800 pages. About $60. Cambridge University Press, NY; (914) 937-9600 or (800) 872-7423. In NY, (800) 227-0247.
4. *Electronic Design*, Penton Publishing. To apply for a free subscription, write to Electronic Design, Reader Service Dept., 1100 Superior Ave., Cleveland, Ohio 44197-8132.
5. *Popular Electronics*, about $19 per year. Call (800) 827-0383 or (516) 293-3000.
6. *Operational Amplifiers: Theory and Practice*, James Roberge, 1975, 678 pages. About $71. Wiley/Krieger. Call (407) 724-9542.
7. *Operational Amplifiers (Second Edition)*, Jiri Dostal, 1993, 555 pages. Butterworth-Heinemann, Stoneham, MA. Available from Robert Pease for $53, including tax & shipping. (see address in reference 1)
8. *Intuitive IC Op Amps*, Thomas M. Frederiksen, McGraw-Hill, 1988, 352 pages. Order from Thomas Frederiksen, 24705 Spanish Oaks, Los Gatos, CA 95030; $25.00 including tax & shipping.
9. *Operational Amplifiers Databook*, National Semiconductor Corp., 1993. Publication No. 400061.
10. Analog Devices Inc., Literature Dept. (617) 461-3392.
11. *Linear Applications Handbook*, National Semiconductor Corp., 1994. Publication No. 400043.
12. *Power ICs Databook*, NSC 1993. Publication No. 400062.
13. *Data Acquisition Databook*, NSC, 1993. Publication No. 400033.
14. *Linear Application-Specific ICs Databook*, NSC 1993. Publication No. 400060.
15. Set of 5 NSC linear databooks—items 9, 11, 12, 13, and 14 above—call the NSC Customer Response Center, (800) 272-9959 or (817) 468-6811.
16. *World Class Quality: Using Design of Experiments to Make It Happen*, Keki R. Bhote, AMACOM, 135 W. 50th St. NY, NY 10020; (518) 891-5510 About $25.
17. *Statistical Problem Solving—A Team Process for Identifying and Resolving Problems*, Hans Bajaria & Richard Copp, 1991, 300 pages. About $45. Multiface Publishing Co., Garden City, MI; (313) 421-6330.
18. *Statistical Methods for Testing, Development, and Manufacturing*, Forrest Breyfogle, John Wiley & Sons, 1992; (908) 469-4400. About $65.
19. *Practical Experiment Designs for Engineers and Scientists*, William Diamond, 1981, 347 pages. Van Nostrand Reinhold, NY. About $55. Call (800) 842-3636 or (606) 525-6600.
20. *Handbook of Analog Circuit Design*, Dennis L. Feucht, 1990, 685 pages. About $65. Academic Press/Harcourt Brace Jovanovich, San Diego, CA; (800) 782-4479 or (407) 345-2500.
21. *High-speed Digital Design (A Handbook of Black Magic)*, Howard Johnson and Martin Graham, 1993. About $47. PTR Prentice-Hall, Englewood Cliffs, NJ; (206) 556-0800.
22. *ESD from A to Z*, John Kolyer and Donald E. Watson, 1990, Van Nostrand Reinhold, NY; (800) 842-3636 or (606) 525-6600. About $47.
23. *Electronic System Design: Interference and Noise-Control Techniques*, John R. Barnes, 1987, 144 pages. About $48. Prentice-Hall, NY; (800) 947-7700 (out of print).
24. *Noise Reduction Techniques in Electronic Systems*, (2nd edition), Henry Ott, 1988, 426 pages. About $65. John Wiley & Sons, NY; (908) 469-4400.
25. *High-Technology Degree Alternatives*, Joel Butler, 1994, Professional

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Publications, 1250 Fifth Ave., Belmont, CA 94002; (415) 593-9119. About $22.

26. *ChronDisp I: The Gun From The Past*, Geoff Harries, 1993, Munich, Germany. Can be ordered on a high-density IBM-compatible floppy disk for $4.00 (including tax & shipping) from Robert A. Pease, 682 Miramar Ave., San Francisco, CA 94112.

27. *Scientific American*, about $36/year. Call (800) 333-1199 or (515) 247-7631.

28. *Discover*, Family Media, NY. About $27/year. P.O. Box 420105, Palm Coast FL 32142; (800) 829-9132.

29. *Machine Design*, a Penton Publication. Write on letterhead to 1100 Superior Ave., Cleveland Ohio, 44114-2543.

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2) An eyeglass repair kit.

3) A length of telephone cord with a plug adapter. The hotel gives you a table and chair, but they are usually across the room from the telephone.

4) A styptic pencil.

5) Shoelaces.

6) A small flashlight. I never carried one until lightning hit the transformer in front of a Holiday Inn where I was staying in Florida. They had to evacuate the place in the pitch dark. There was no emergency lighting and the management passed out matches. When you need a flashlight, you really need a flashlight.

7) Rubber bands, safety pins, cable ties, and Band-Aids.

WALTER E. GATELY
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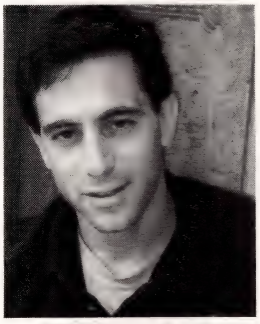
PC GRAPHICS WATCH

VESA FORGES VAGI

GARY WAYNE, ITHACA SOFTWARE

Recently, over 50 companies representing both the hardware and software industries met to develop a new graphics interface standard: the VESA Advanced Graphics Interface (VAGI). Given the number of existing graphics standards, however, it's not unreasonable for board developers to ask "Who needs another graphics standard?"

Although many graphics standards do exist, each tends to focus on a specific aspect of the overall graphics market. In addition to the usual differences that might arise among competitive computer architectures, operating systems, and graphical user interfaces, existing graphics hardware differs greatly in functionality and architecture. Without a common foundation, the market might well remain fragmented and underdeveloped. This is where the VAGI standard steps in.



Graphics, as opposed to some other type of displayed information like video, refers to the synthetic generation of computer pictures from underlying geometric models. The high-end of this market is characterized by CAD, scientific visualization, and photorealistic animation. These typically use floating representations and run on workstations or high-end PCs with specialized graphics accelerators. High-end computer graphics is commonly computed through a series of steps using specialized hardware, software, or a combination of the two. Three-dimensional models are represented by sets of bounding surfaces which are, in turn, defined by the vertices of model edges or the edges of curved surfaces.

The principal operation in 3D computer graphics is the projection of this bounding geometry through an imaginary display surface to the user's eye. Arbitrary model orientation, observer position, viewing direction, and type of projection (such as orthogonal or perspective) can be represented as a series of linear transformations (four-by-four matrix multiplies). By varying these transformations, a continuous motion of objects can be created. The projected geometry must be clipped to the edges of the physical display, or more commonly, to screen windows. Projection and clipping is compute-intensive and often bound by floating-point performance.

If only the bounding edges of the model are projected, the resulting image looks like a transparent wireframe model. To represent solid objects, the surface, rather than just the edges, must be projected and clipped. Human perception of surface orientation, on a page, screen, or in the real world, is based on the variation of reflected light from a surface. For example, the human eye can differentiate between a 3D ball and a 2D circle because the ball typically has one or more bright areas surrounded by dimmer areas.

Because it obviously isn't clear which surfaces or parts of surfaces will be visible to the human eye, hidden surfaces must be computationally removed. Hidden surface removal is accomplished either by various sorting techniques or by using a z-buffer (more common on high-performance systems). Z-buffers store per-pixel depth values and pixel color. As new surfaces are painted to the screen or z-buffer, depth values are compared and the closest surface color is retained. By using an extra alpha buffer, the effect of transparency and translucency can be approximated by accumulating net pixel color based on its orientation and the transparency values assigned to each surface. Other techniques also can enhance picture quality, including pixel blending to simulate continuous straight lines across discrete pixels (antialiasing); application of realistic surface properties (texture-mapping); and attenuating brightness to simulate depth (depth-cuing).

One goal of the technical committee is to define a non-proprietary, royalty-free interface to support advanced graphics that's independent of the operating system, window manager, graphics device, and applications program interface (API). In addition, support for game and entertainment software development for unaccelerated systems will be examined. For example, the low-end of the PC market is often driven by systems that contain unaccelerated graphics hardware.

One key design goal for the VAGI is scalability. In addition to giving software developers a constant set of capabilities across devices, the VAGI must make different levels of its graphics pipeline available. This must be done in a way where designers can opt to accelerate particular elements of the standard, depending on the price-performance requirements of their target markets.

The VAGI technical committee should have a draft specification and sample implementation running by May. For additional information, contact the VESA office at (408) 435-0333.

Evaluating Embedded Systems Performance

Applying multiple parallel processors is one way to increase system performance.

BY D. DOUGLAS WILMARTH
Sky Computers Inc., 27 Industrial Ave., Chelmsford, MA 01824, (508) 250-1920.

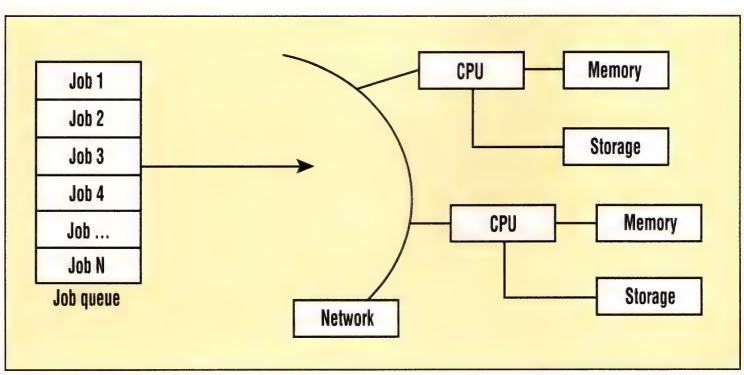
Design engineers and developers are continuously faced with the challenge of making their products faster, better, and cheaper, as well as delivering them to market quicker. One alternative to designing an embedded system from the ground up is to leverage the availability of commercial off-the-shelf (COTS) computer hardware. However, board-level COTS computers can more easily meet the required performance level by employing parallel-processing techniques. Because there are other alternatives, engineers/developers must determine which COTS hardware configuration and programming model will be most efficient for their application.

The hardware architectural features typically used by COTS vendors to optimize performance are interconnect topology, memory locality, and synchronization facilities. Each of these features makes a different contribution to optimum performance.

Memory locality. Bandwidth between the processor and the memory system govern how fast the innermost calculations can be performed and ultimately how fast the application runs. Where the memory is physically located with respect to the processor will govern this speed. Whether memory is globally addressable or strictly local will determine how visible the interconnect topology will be to the programmer and how much hidden contention exists with other processors.

Synchronization facilities. How the processors alert other processors of their status is an important issue for avoiding deadlocks. Simple coordination at the network level is usually done in the operating system using pipes, sockets, messages, and semaphores. The lower the programming level needing synchronization, the more likely that a hardware solution will be required. Architectures employed in machines developed by MasPar and Thinking Machines Corp. have built-in synchronization because there's only one instruction stream. Architectures like those found in Cray and Convex systems have separate buses that are built with synchronization registers.

Interconnect topology. The type and number of connections between processors and how they interact determines how fast information gets processed. Communication speed and bandwidth are performance-governing characteristics. Many different topological configurations have been productized over the years to improve these characteristics. Each topology offers its own benefits that fit a particular application. Some vendors even let their customers build their own application-dependent topology. This is considered a "roll your own" approach, and it requires considerable system-design resources *(see "Interconnect Topology Options," p. 94).*



1. The job stream in the symmetric-multiprocessing (SMP) system can range from one job up to hundreds. In addition, the CPU can consist of mainframes, supercomputers, or even workstations. The CPUs connect to the job stream over a network link.

To take full advantage of hardware architectures and multiple processors, developers must select the most effective parallel-programming model for their application. Parallel processing has long been touted as the panacea that supplies true scalability for multiprocessor architectures. However, choosing the right parallel paradigm, like choosing the right hardware architecture, requires careful analysis.

Job-level parallelism, the most prevalent form of parallel processing, is the classic model of an MIS Data Center. Each job is executed on one processor—no data or code is shared and no interprocess communication is needed. A symmetric-multiprocessing (SMP) architecture is characterized by a general-purpose CPU architecture that integrates seamlessly with new additional systems.

This is one of the more efficient approaches to parallelism. However, two conditions must be present: the amount of resources required by an individual job is a small portion of a single uniprocessor, and the nature

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INTERCONNECT TOPOLOGY OPTIONS

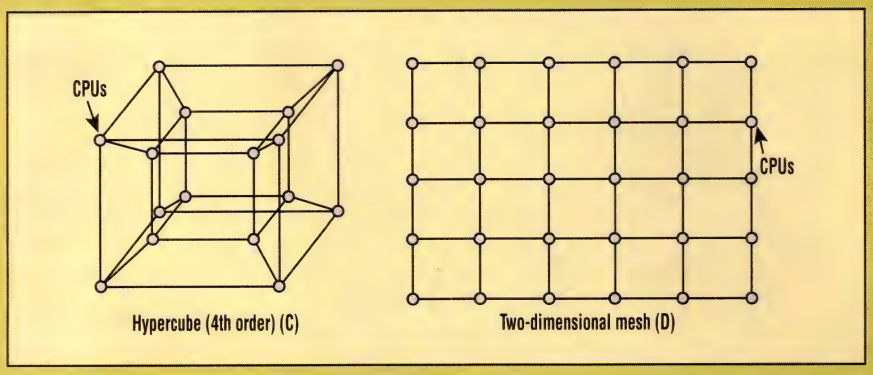
Different interconnect topologies are suited for particular applications. For high-end systems, some of the popular types include:

Bus-connected: Each processor is connected into a common communications pathway, or bus, that's used by all processors *(Fig. A)*. Because the bus and processor designs are entirely independent, this is the simplest approach. And because all communications pass through a single pathway, there's a limitation beyond about ten processors. Though multiple processors share common peripherals and resources, very little communication exists between them. The bus-connected architecture has been successful in the server-type environment.

Token ring: Each processor in the ring is connected to a network where multiple, concurrent transfers can be accommodated *(Fig. B)*. The transfers only affect the section of ring that's in use; other transfers can employ other sections of the ring.

Token-ring networks were explored extensively by IBM. Although it's an improvement over the simple bus, conversations between nodes separated by a substantial "distance" (a large number of intermediate nodes) significantly degrades the overall performance of the ring.

Hypercube: The hypercube topology can be viewed as a cube with processors at each corner. With eight processors, each processor has three connections, one to each of the nearest neighbors. If the number of processors is 16, each has four connections *(Fig. C)*. Doubling the number of processors adds another connection to each, so that a 1024-processor design would have ten connections for each processor.



The first large-scale parallel systems to market were hypercube designs. These can also be found in high-end machines, such as the Thinking Machines CM-2, the Intel iPSC-860, and the nCUBE-2. In actual real-world applications, the hypercube only is used along a subset of the available connections, reducing the system to a ring, mesh, or tree topology. While architecturally elegant, the cost of the interconnects increases faster than the number of processors, making the high-end configurations proportionately more expensive than the lower-end ones.

Meshes: The two-dimensional mesh evolved from the hypercube. Here, each processor can talk to the four nearest neighbor processors in a grid configuration *(Fig. D)*. The advantage of the mesh architecture is that the connection costs scale linearly with the cost of the processors.

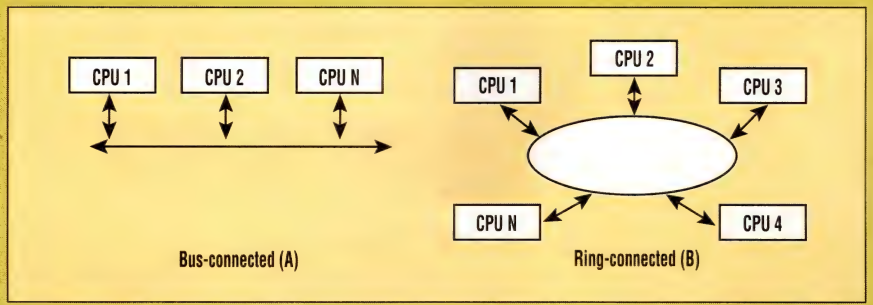
For two-dimensional applications, such as image processing, the mesh offers a good solution. But the programmer must be aware of this topology to properly exploit it. Vendors also have experimented with three-dimensional meshes, where each processor has six nearest neighbors.

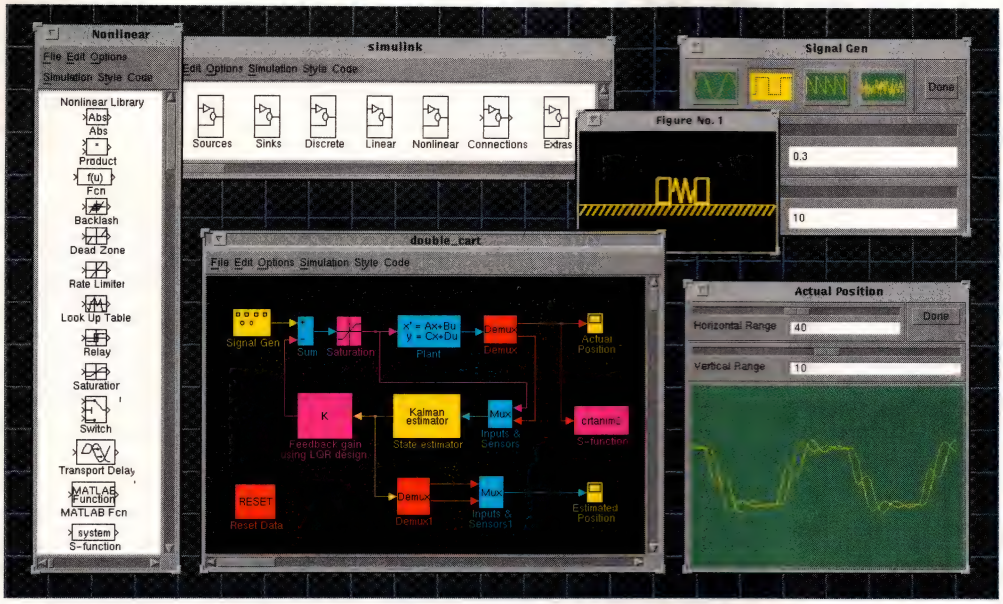
Trees: The tree topology resembles an inverted hypercube, where each node is an end-point. Local nodes are connected by a crossbar to each other and to an external port. In addition, external ports connect to each other through crossbars.

Like the hypercube, the tree topology can be idealized as a bus, ring, or mesh. But the cost of the interconnect scales faster than the number of processors. Hence, this architecture becomes uneconomical if a large number of processors is needed.

Hierarchical and heterogeneous: To maximize performance, each of the aforementioned topologies can be implemented at an appropriate level in the hierarchy. Between processors and clusters of processors, crossbars supply the required bandwidth and present the most cost-effective solution. Communication requirements from board to board can be handled easily with buses.

From chassis to chassis, a network approach is the most effective alternative. This becomes a layered architecture, or hierarchy of crossbars and buses, with each layer having an appropriate capacity to its level in the system. Overall performance is improved because the optimum solution is implemented for each step.





Simulating a system with SIMULINK: Scope block and MATLAB animation window show results while the simulation is running. You can change parameters during a simulation to do "what if" analyses.

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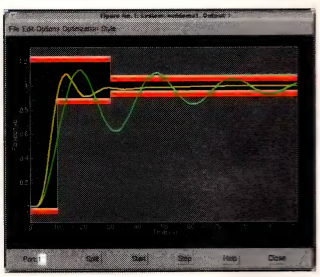

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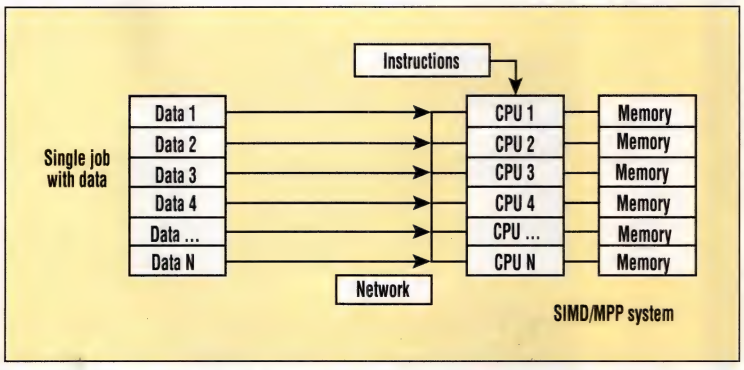
of each job is substantially different from others in the job stream. In this processing model, each processor takes the next task in the queue, completes it, then goes on to the next one. Processors need to be added as the volume of work goes up, but they can be of differing capability, size, and performance (heterogeneous).

There may be significant system resources and sections of the operating-system code that are shared between the processors. In most cases, the OS supports multiple jobs on each processor in a multitasking mode. The interconnect topology includes everything from LANs to high-speed buses and crossbars. The main memory is always local to the processor and the synchronization facilities are always at the OS level. The job stream allows for one to several hundred users. The CPUs can be mainframes, supercomputers, and/or workstations *(Fig. 1)*

SIMD (single-instruction, multiple-data) designs are homogeneous collections of functional units sharing a common instruction unit. All units are available for use on each job. In most cases, the synchronization facilities are fixed—all of the units work in parallel in lock-step fashion. The interconnect topology between the functional units is used for data communication.

A significant amount of government and university research has targeted data-level parallelism. Typically, thousands, even millions, of jobs need to be done, and each is nearly identical to the next. It differs only in the data set supplied. One processor is employed for each data set, reducing the run-time for many jobs down to the time equal to just one. Imaging applications are suitable for this model, where one CPU is allocated to each output pixel.

Massively-parallel-processing (MPP) designs attempt to be more general-purpose than



2. In a single-instruction, multiple-data (SIMD) or massively-parallel-processing (MPP) system, each CPU has access to each piece of data. The processors each have their own local memory.

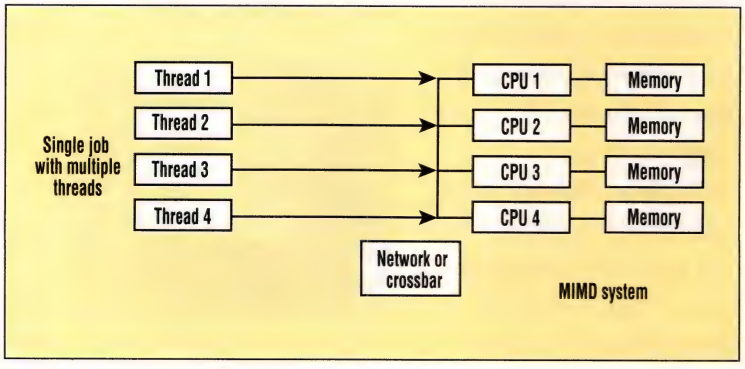
SIMD designs. The MPP system is still homogeneous, but each node is a full CPU, not just a set of functional units. Each CPU contains its own set of instructions that need to be coordinated with the cooperative processors. Theoretically, a job should be able to dynamically request an arbitrarily large set of processors, execute time-critical sections, and release them to other jobs when not in use. The difficulty here is that the synchronization facilities need to be closely associated with the CPUs to be effective. While very efficient at the supercomputer level, this paradigm isn't practical for embedded applications *(Fig. 2)*.

In applications like sonar, radar, or signal processing, the algorithms have natural partitions or "threads" that can be delegated easily and the results collected efficiently. The multiple-instruction, multiple-data (MIMD) system is a collection of nearly independent processors with each running a separate thread of a single job. The processor handling each thread carries data in a local memory, and thus it usually needs access to the shared (global) data.

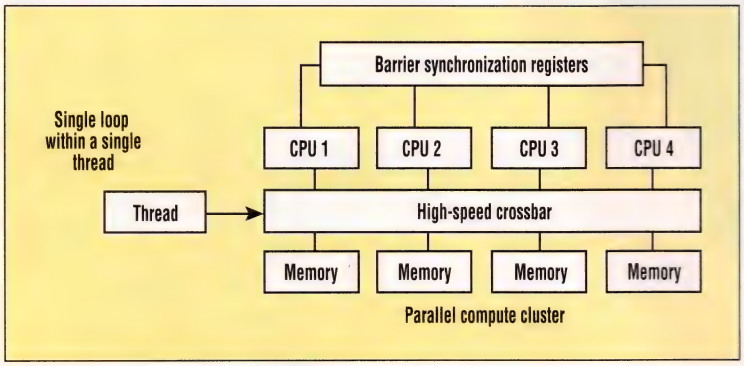
The ratio of local to global data accesses determines the speed and extent of the hardware-interconnect topology and the synchronization facilities. A high ratio (lots of local memory and no global memory) will permit most topologies to work, even with small bandwidths, and there's few synchronization requirements. However, a low ratio (small amount of local memory and lots of global memory) will stress even the most robust designs.

The level of parallelism can be defined as small, medium-size, or large. These groups require very little communication during critical operations because each processor has its own set of instructions to follow. However, they all need much preparation to operate in the most efficient manner *(Fig. 3)*.

The MIMD system has the same characteristics. A significant amount of time is spent distributing the data in separate memories for parallel code execution. The threads assigned to each processor need to run for extended periods of time with



3. The multiple-instruction, multiple-data (MIMD) system consists of a collection of nearly independent processors. Each processor handles a separate thread of a single job.



4. Loops of data are automatically parallelized across all processors within a cluster in the parallel-compute cluster of an single-program, multiple-data (SPMD) system.

little or no communication to other threads or the overhead will outweigh the improvement. At some point, all of the threads must be brought back together to complete that task. The amount of the various overheads defines what types of applications will run best.

MIMD best addresses simulation applications, like weather modeling or aerodynamics. The data sets have large quantities of local computation that can be processed independently, but a collection step must first be efficiently completed by intelligent processors. This partitioning problem isn't trivial, and must be built into the application's basic structure. It also implies that tuning this type of solution depends on the number of processors, the coding style, and the availability of development tools, such as compilers, profilers, and debuggers.

Loop-level represents the lowest level of parallelism, and it has the most stringent hardware requirements. Multiple CPUs process a single loop cooperatively within a section of code. The hardware interconnect topology must permit easy access to each memory location concurrently from all processors, essentially making all memory local. The synchronization facilities must permit coordination between processors in a minimum of cycles, because the time spent by each processor in its section of the loop may only be a few hundred cycles.

A full crossbar switch gives every processor access to all sections of memory. Multiple accesses to the same memory bank are serviced in a round-robin fashion so that no processor can be locked out. Arbitration occurs entirely in hardware. Coordination between the processors happens through barrier-synchronization registers, which are mapped directly into the executive running on the compute processor. The registers can be accessed without going through the crossbar.

Using these hardware features, the single-program, multiple-data (SPMD) programming model can be extended to the parallel-compute cluster model *(Fig. 4)*. This automatically parallelizes loops across all processors in the cluster.

D. Douglas Wilmarth, the director of major programs at Sky Computers, received a BSCE from Northeastern University in Boston and an MSCE in structural design and a Degree of Engineer in structural mechanics from Stanford University in California.

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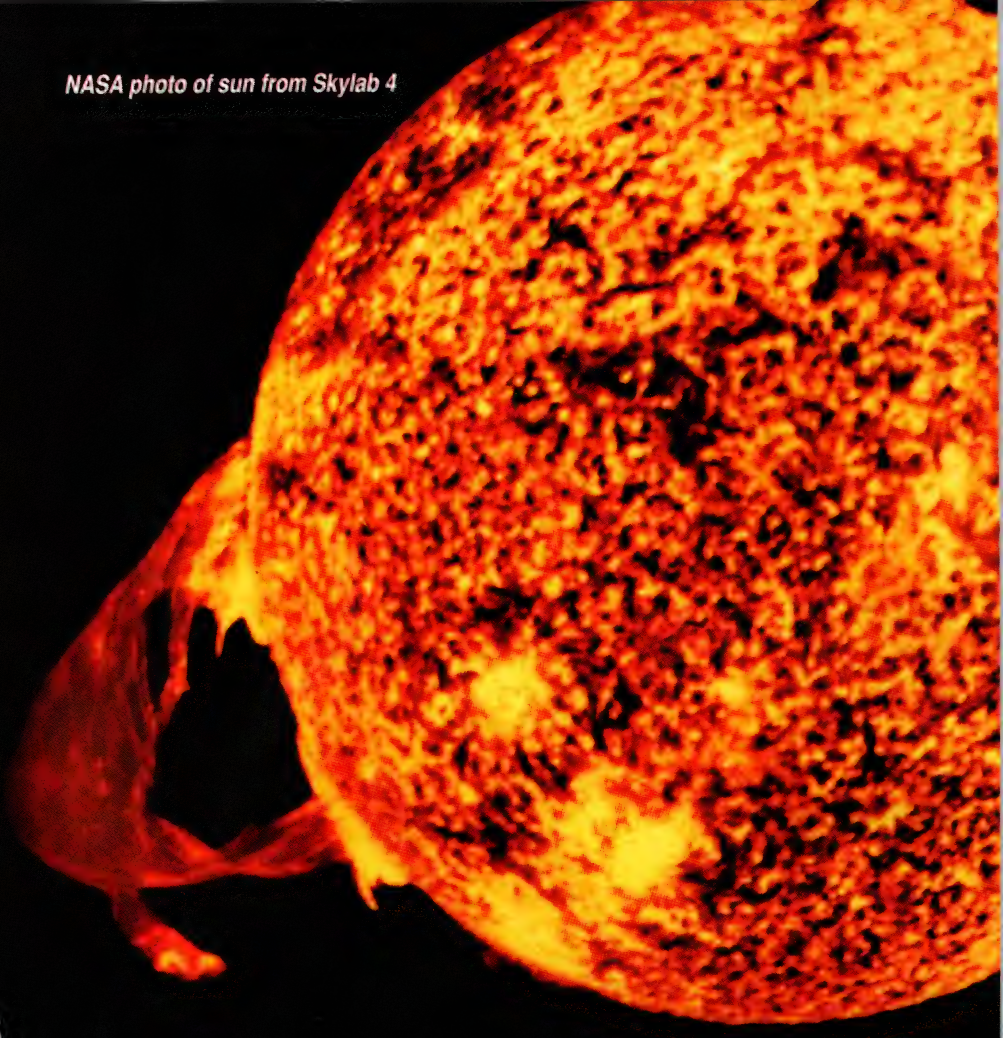

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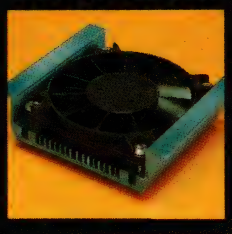

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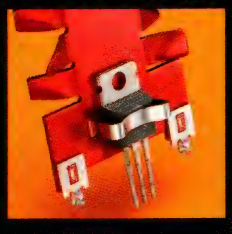

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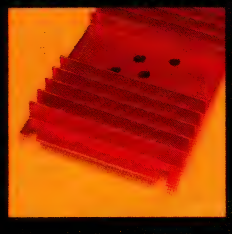

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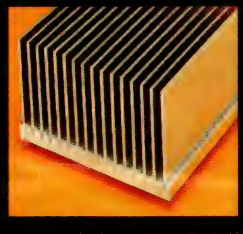

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SYSTEM DESIGN NEWS

A family of clock buffers, operating at over 100 MHz, can support the varied timing requirements of such processors as the R4000, the i486, the Pentium, and others. The GA1085, 1087, and 1088 from TriQuint Semiconductor, Santa Clara, Calif., keep output-to-output skews under 150 ps. The buffers come in two propagation-delay options—one with a nominal 350 ps ±500 ps (maximum) and the other with a tolerance of ±1000 ps. The first option is aimed at high-speed synchronous multiprocessor systems, while the lower-cost second option targets uniprocessor designs. Each buffer provides 11 outputs, with each chip offering a different configuration. For instance, the GA1085 includes an on-chip phase-locked loop and an on-chip divider that lets it deliver outputs that are 1× and 2×, or 1× and 0.5×, the reference clock frequency (f_{REF}). The output configuration can be set as four outputs at f_{REF}, four more at $f_{REF}/2$, and two outputs at $f_{REF}/2$ with adjustable phase. An alternative configuration for the same chip sets up five outputs at double f_{REF}, three outputs at f_{REF}, and two at f_{REF} but with adjustable phase. Selectable phase shifts allow compensation to be added for trace delays. The buffers are housed in 28-lead metal quad-sided flat packages, and include TTL-compatible output drivers that deliver up to 30 mA for heavy loads. Prices start at $16 apiece in lots of 10,000 units. Contact Sunil Sanghavi at (408) 982-0900.

An inexpensive scheme for printer sharing and a utility for networked E-mail now makes these capabilities attractive for small workgroups or home offices. MosesSPOOL!, a printer-sharing solution from Moses Computers, Los Gatos, Calif., comes as a two-user starter kit. The kit includes two cards that each plug into a PC, a 25-ft. cable, and the spooling software. Each PC that has an attached printer then becomes a print server and that printer can then be used by either computer. Transferring data at 2 Mbits/s, MosesSPOOL! operates 10 to 40 times faster than most other printer-sharing solutions. Its spooling utility allows users to do other tasks on the PC while the printer is operating. The system also can be enhanced to serve as a full Moses LAN with just a software upgrade. A basic printer-sharing starter kit goes for $179. MosesCALLS! provides a terminate-and-stay-resident program that permits screen-to-screen communications on a Moses LAN from within DOS applications. In addition, it lets users create the equivalent of up to 14 "yellow sticky" notes on the screen. The software also includes a call log that date-and-time-stamps calls entered into the log and allows for a "group chat" with up to four users. Contact Moses Computers at (408) 358-1550.

A family of multifunction mouse controller chips lets designers control serial or IBM-compatible PS/2-style mice. Developed by Hualon Microelectronics, the HM8450/1/6/7 handle three key-switch inputs and four photocoupler inputs, feeding the information directly to an RS-232C serial port. Using the various options available with the chips, designers can implement optical, pen, mechanical, and optomechanical mice. They can also implement optical, mechanical, and optomechanical trackballs. The low-power chips, which use an inexpensive 32.768-kHz crystal, can be powered from the RS-232 cable in the serial mode. In the PS/2 mode, the chips can receive a command and echo status or data. On-chip key-debouncing circuitry prevents phantom data entries, and high-noise-immunity circuitry minimizes the effect of noise. The chips' auto-speed adjusting circuits make for very smooth cursor operation when the mouse moves slowly. When the mouse is moved at high speeds, though, the controllers can adjust to move the cursor quickly across the screen. Chip options include the ability to set modes or data-transfer rates of 1200 or 9600 baud, or operate in either a Microsoft- or Mouse Systems-compatible mode. All versions come in 18-lead small-outline plastic packages and sell for under $1.75 each in lots of 10,000 units. Call Louis Gerhardy of the Summa Group Ltd., San Francisco, Calif. at (415) 288-0390.

▼ INDUSTRIAL PC WITHSTANDS EXTENDED TEMPERATURES

Built with a 50-MHz 486SLC microprocessor, the 5050 Micro PC is a miniature CPU board designed for industrial applications. The board can handle temperatures ranging from –40 to +85°C. The 5050 board operates from a single 5-V supply in a standalone configuration or in a multi-card, passive-backplane system. A keyboard and monitor aren't required. The CMOS construction consumes under 1.5 W, eliminating the cooling fans in most environments. Three solid-state disks are included: the first holds the operating system, the second has 512 kbytes of flash memory for program storage, and the third disk contains 1.5-Mbytes of battery-backed RAM for logging data and process variables. There's also room on the board for 4 Mbytes of system DRAM. Other features include one parallel and two serial ports and a clock-calendar. The 5050 sells for $895.

Octagon Systems Corp.
6510 W. 91st Ave.
Westminster, CO 80030
(303) 430-1500
▶ CIRCLE 601

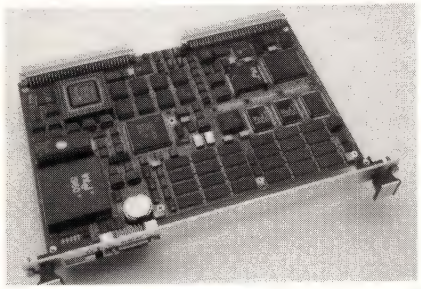
▼ PCMCIA CONTROLLER ADDS PLUG-AND-PLAY SUPPORT

Designed to support the growing Plug-and-Play initiative, the DB86084 is a single-chip, PCMCIA interface controller. The controller supports two electrically-isolated PCMCIA sockets in a single-voltage environment. Each Plug-and-Play device is identified and configured by the system through software at boot up. The DB86084 can eliminate an external EEPROM that typically stores the resource data, reducing the required board space. For systems that need more than two slots, up to eight controllers can be linked together while still maintaining full Plug-and-Play compatibility. The DB86084 is available now with an evaluation board (model TMI-160). Software support is also available, including the company's ExCA-verified CardTalk 3.0 utility.

Databook Inc.
Tower Bldg., Terrace Hill
Ithaca, NY 14850
(607) 277-4817
▶ CIRCLE 602

▼ BOARD TARGETS GRAPHICS, COMMUNICATIONS

The HK80/V960D CPU board, which holds up to 16 Mbytes of parity-checked DRAM, 4 Mbytes of flash memory, and 512 kbytes of ROM, is designed around a 32-bit 80960CF

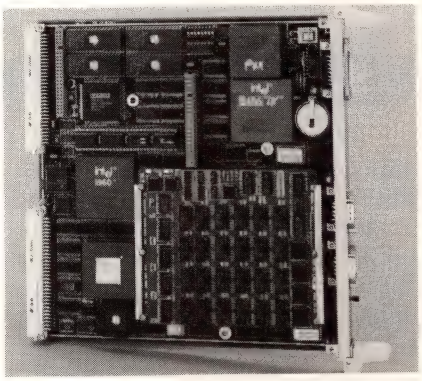


RISC processor. The 30-MHz board is aimed at communications or graphics-oriented applications that require high-speed I/O and memory-to-memory data transfers, such as printing, image processing, and simulation. It features a 54-Mbyte/s VME64 system-bus interface and a 32-bit, 200-Mbyte/s mezzanine bus called Corebus, and can perform memory-to-memory transfers at rates of 60 Mbytes/s. The board also contains on-board Ethernet, four serial ports, and a real-time clock with 512 bytes of battery-backed RAM. The VxWorks real-time operating system is supported. Available immediately, the HK80/V960D costs $4495 with 8 Mbytes of DRAM.

Heurikon Corp.
8310 Excelsior Dr.
Madison, WI 53717
(608) 831-5500
▶ **CIRCLE 603**

▼ MULTIBUS II BOARD HOLDS DUAL PROCESSORS

Multibus II users can get both high performance and high functionality from the CP 486/ES2 board. Such high performance comes from the combination of a 66-MHz 486DX2 processor and a 33-MHz 960CA CPU. The 960 acts as a DMA and I/O controller to maintain efficient message-passing across the Multibus. Consequently, the host 486DX2 chip has more bandwidth for application processing. A 33-MHz 486 version is



also available. The functionality is a result of the various interfaces on the board, including SCSI, Ethernet, and two serial ports. In addition, two iSBX expansion interfaces can hold customized I/O options. The board holds up to 64 Mbytes of DRAM using low-profile memory modules. There's also room to install up to 4 Mbytes of EPROM or flash memory.

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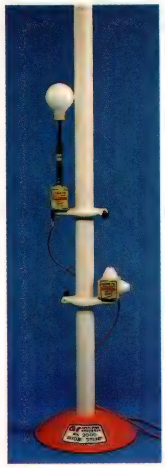

84-inch probe stand (easily cut to lower height) lets you position probes where you want them. One screw clamp included with each stand, additional clamps available.

The FM2000 accommodates up to four probes of either or both frequency ranges, for placement at various locations in the shielded room. Each probe delivers its own signals through an input card to the control console, and you can select HI/LO/AVG readings from multiple probes at the touch of a finger on the keypad. Outputs are provided to IEEE-488 and RS-232 interfaces and 0-4 Vdc, giving you the widest choice for automatic field control — plus audible signal and SPDT contact closure for excessive-field-level or low-battery alarm.

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6313

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SYSTEM DESIGN PRODUCTS

▼ EIGHT-CHANNEL MODEM ADDS ADCPM COMPRESSION

The MM9624 eight-channel modem comes with ADPCM voice compression. Because the modular modem sends and receives faxes at 9600 baud and data at 2400 baud, a PC can service all eight models in parallel. Each modem is fully independent with its own CPU and DSP chip. The performance of the combined units exceeds 256 MIPS. The modems are built with a 16550 parallel FIFO buffer and its associated high-speed driver, and are compatible with such operating systems as Windows and OS/2. Integrated logic permits use of just one communication address, rather than the four that are typically required.

Advanced Micro Technology Inc.
123 University Pkwy.
Pomona, CA 91768
(714) 598-6120
▶ CIRCLE 605

▼ FLOPPY DRIVE PLUGS INTO PCMCIA SLOT

The 2000 Series portable floppy-disk drive connects to a computer through its PCMCIA slot. The 3.5-in. form factor drive comes complete with the PCMCIA-card connection, cable, and power supply. Because

floppy disks are relatively inexpensive, this setup can become an alternative to employing flash-memory cards. No software drivers are required. The driver issues are handled using the card-socket services of the PCMCIA slot. The unit is compatible with the latest PCMCIA standards and fits in a Type II slot. Available now, it sells for $399.

Yaskawa Electric America Inc.
2942 MacArthur Blvd.
Northbrook, IL 60062
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▶ CIRCLE 606

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▼ NUBUS SCSI-2 BOARD PUSHES 20 MBYTES/S

Designed for NuBus-based computers, the SiliconExpress IV is a SCSI-2 accelerator card that speeds such applications as digital video and file servers that require high SCSI throughput without lots of overhead. The board, which fits into Macintosh, Quadra, Performa, and Centris systems, supports sustained 16-bit, SCSI-2, 20-Mbytes/s data-transfer rates. Each board can handle up to 15 SCSI bus IDs without disabling the built-in SCSI port. Other features include bus mastering and bus throttling, NuBus-to-NuBus interboard support, and zero wait-state block-mode transfers. Available now, the board sells for $995. An OEM developer's kit is available for custom programming.

ATTO Technology Inc.
Audubon Technology Park
40 Hazelwood Dr. #106
Amherst, NY 14228
(716) 691-1999

▶ **CIRCLE 607**

▼ MECHANICAL KEYBOARD IS 22% SMALLER

The RT-8700 series keyboard offers a footprint that's 22% smaller than standard mechanical keyboards, yet maintains industry standards for

spacing between keys. The keyboard gives users the "click" feel by employing a mechanical clicker key switch. In addition, the unit is certified to be compatible with the Novell Netware operating system. Cabling can be routed from the back of the keyboard in any direction. The RT-8700, with dimensions of 18 by 6 in., is priced at $75.

NMB Technologies Inc.
9730 Independence Ave.
Chatsworth, CA 91311
(818) 341-3355

▶ **CIRCLE 608**

▼ GRAPHICS BOARD EMPLOYS DUAL PROCESSORS

The Dual Lightning graphics-accelerator board employs two independently programmable Tseng Labs ET4000/W32i graphics processor chips. The board, which takes advantage of the high-speed 32-bit VL-Bus, can drive two separate displays simultaneously. Included are 4 Mbytes of DRAM, two for each channel. Resolutions up to 1024 by 768 pixels with 256 colors are supported. With Dual Lightning's software drivers, users can build one virtual display using two separate monitors. This lets users view an entire screen spread over two monitors. The drivers support Windows 3.1 and OS/2 2.1. In large quantities, the Dual Lightning accelerator board sells for $750.

Colorgraphics Commications Inc.
5388 New Peachtree Rd.
P.O. Box 80448
Atlanta, GA 30366
(404) 455-3921

▶ **CIRCLE 609**

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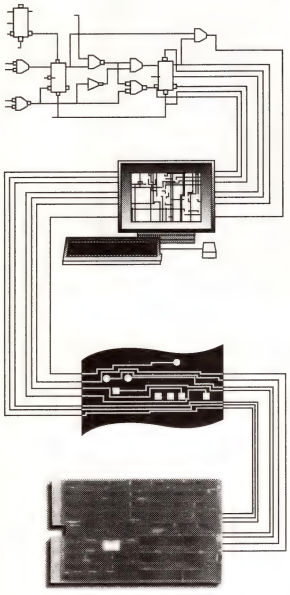

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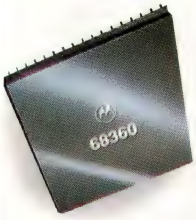

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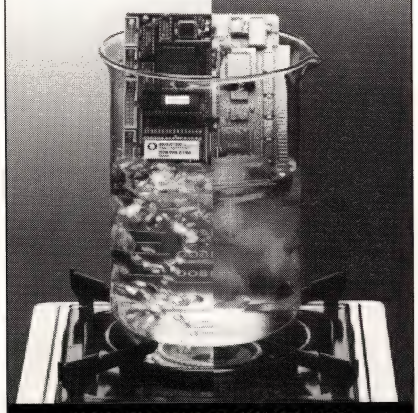

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SYSTEM DESIGN PRODUCTS

▼ ACCELERATOR BOARD PLUGS INTO PCI BUS

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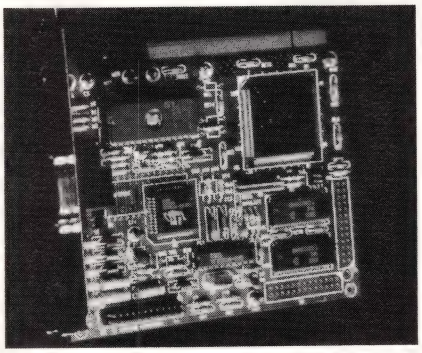


70-ns DRAM to supply up to 16.7 million colors at a resolution of 640 by 480 pixels, and a 60-Hz refresh rate. The Avance controller that forms the brains of the board supplies full hardware support for BitBLTs, line-drawing engines, polygon fills, ellipse fills, and cursor operations. A bundled utility automatically configures the switchless card and installs the drivers on the host. Other utilities are also supplied. Available now, the Express PCI costs $199.

STB Systems Inc.
1651 N. Glenville
Richardson, TX 75081
(214) 234-8750
▶ CIRCLE 610

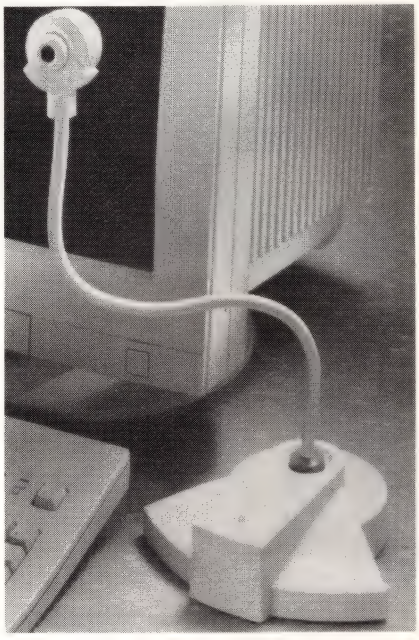
▼ SOFTWARE HELPS BUILD INTERACTIVE TELEVISION

The Digital Audio/Video Interactive Decoder (DAVID) package includes all of the software modules needed to design an MPEG decoder for interactive digital television. At the heart of the package lies Microware's OS-9 or OS-9000 real-time operating system. A Motion Picture File Manager (MPFM) controls the decompression and synchronization of MPEG-encoded digital audio and video. Also included are I/O managers that control wide-area network (WAN) communications, graphic overlays, and infrared remote controls. DAVID can operate with either a Motorola 68000 or Intel 80X86 microprocessor. In addition, drivers are incorporated for a variety of MPEG audio and video decoders, communication interfaces, and graphics ICs. The complete DAVID package, which comes with Microware's Ultra C compiler, a source-level debugger, and a manufacturer's distribution license agreement, costs $75,000. For $25,000, a board package is available to develop a DAVID system decoder in a PC environment.

Microware Systems Corp.
1900 N. W. 114th St.
Des Moines, IA 50325
(515) 224-1929
▶ CIRCLE 611

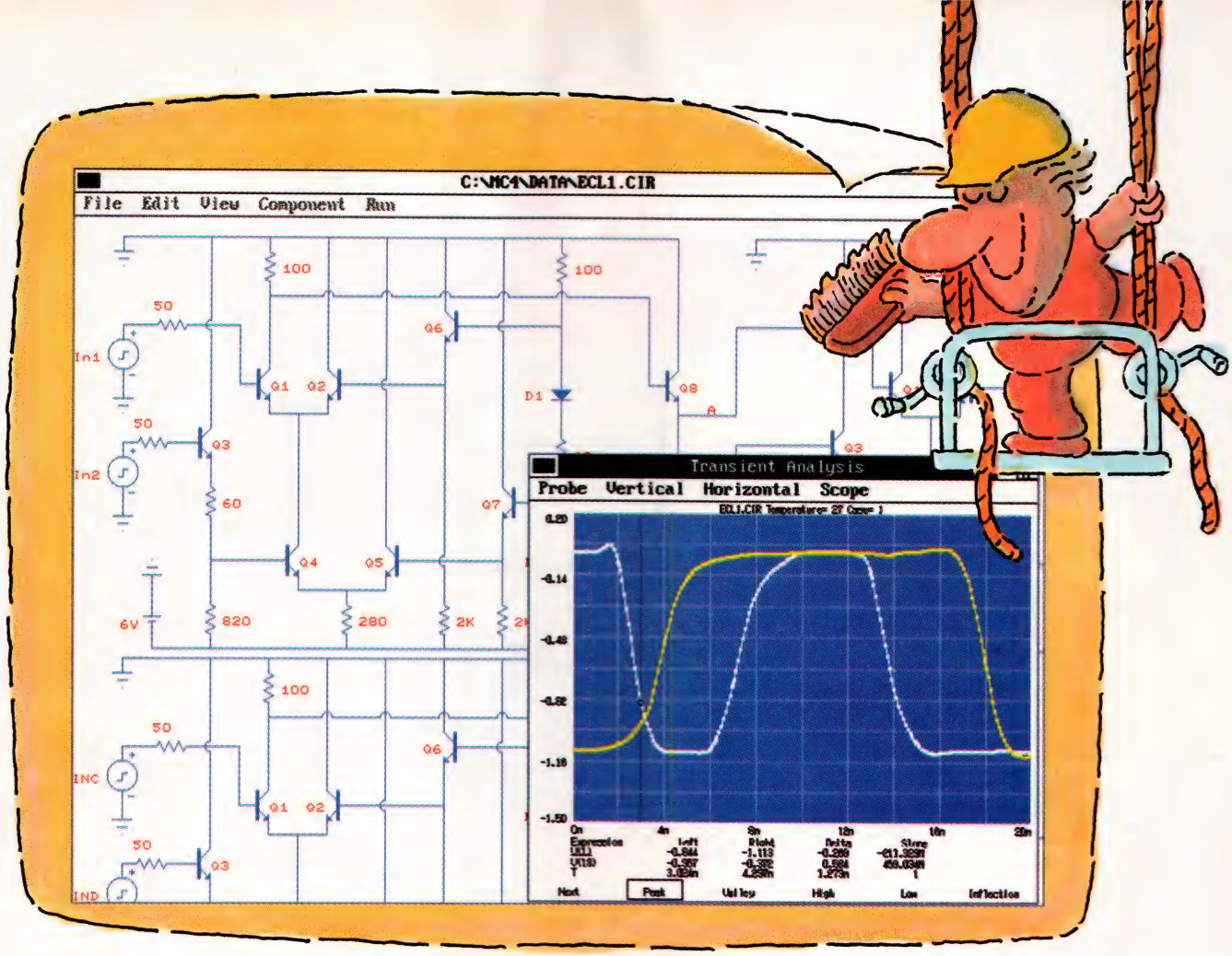
▼ FLEXIBLE CAMERA FITS ON A DESKTOP

Documents now can be photographed or scanned using a low-cost desktop video camera. The FlexCam/Document camera's 8-mm lens can handle images up to 8 by 12 in. with the neck fully extended. In addition, it can be focused down to 1/4 in. to produce a magnification of 50-to-1



when viewed on a 25-in. monitor. Transparencies and three-dimensional objects also can be scanned. The camera's output, which is in an NTSC or PAL format, has more than 270,000 pixels, resulting in 350 television lines of resolution. A mechanical iris corrects the color quality. The FlexCam/Document camera sells for $995; with microphones, it goes for $1045.

VideoLabs Inc.
5270 W. 84th St.
Minneapolis, MN 55437
(612) 897-1995
▶ CIRCLE 612



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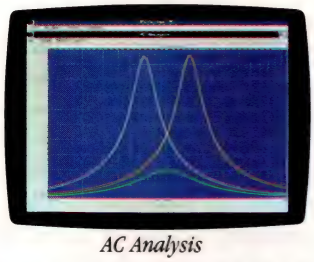

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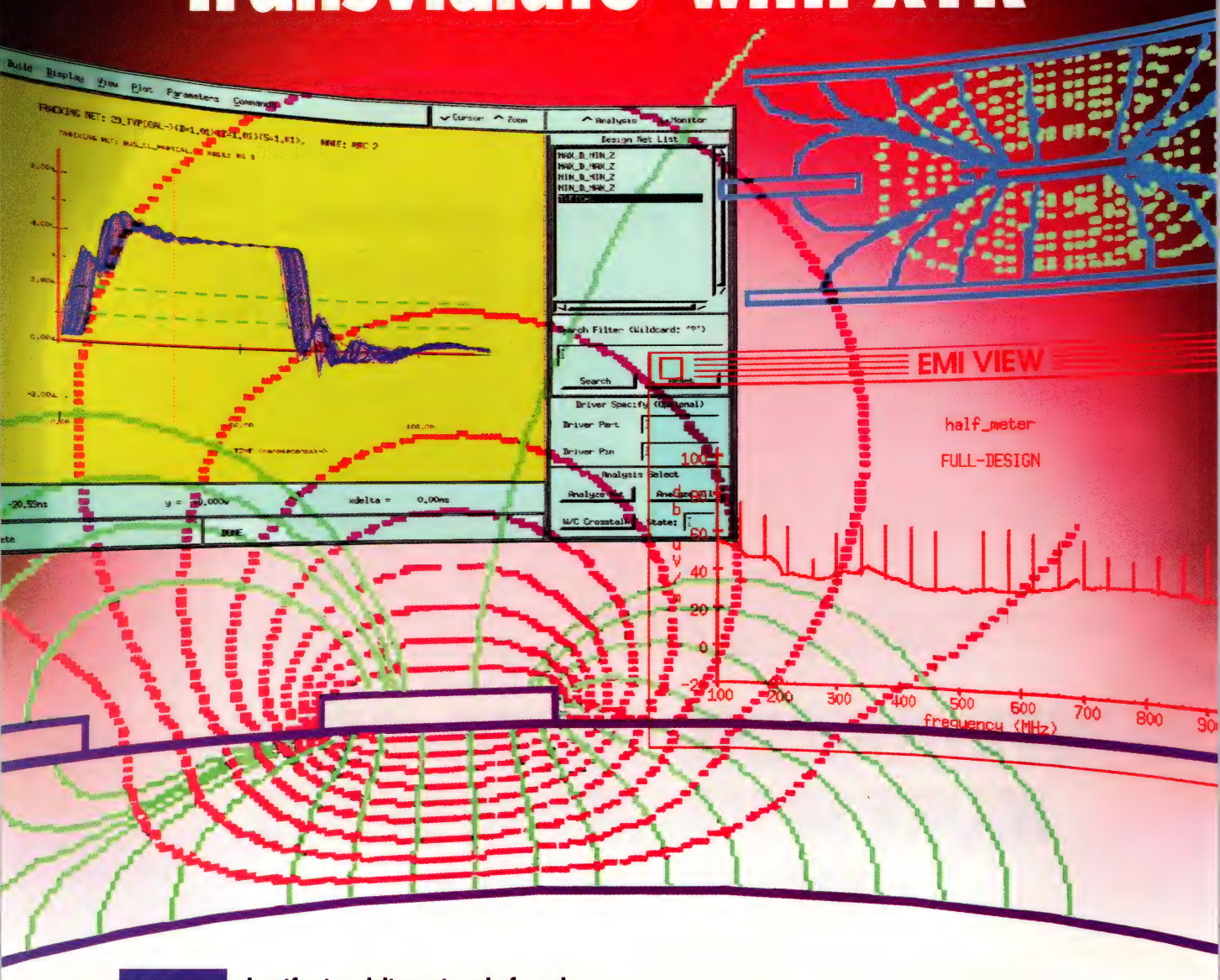

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* ***transvidiate*** *(trans vid'ē āt')* vt. ***-a ted, -a ting*** *[TRANS (L.* across, over*) + VID (L.* videre, *to see) + -IATE)]* ***1.*** *to bridge the present and future by knowing all signal distortion effects of your digital circuit design before they happen* ***2.*** *to avoid future design mistakes while the design is still a vision* ***3.*** *to exist in the future presently* — ***trans-vid'i-a'tion*** n.

READER SERVICE 145

DSP HANDLES SOUND WHILE LINKING AUDIO AND SCSI

16-BIT BUSINESS AUDIO CAPABILITIES ARE IMPLEMENTED ON THE SAME BOARD WITH A FULL-FUNCTION SCSI HOST ADAPTER.

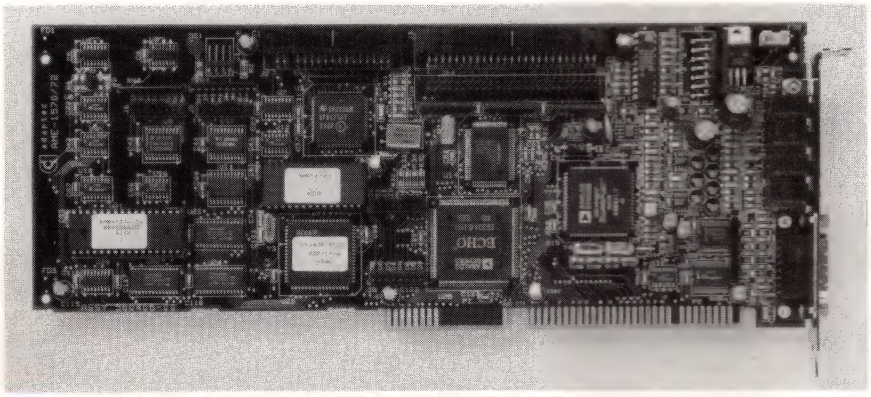
RICHARD NASS

Sound cards aren't just for games anymore. When these boards hit the mainstream PC market a few years ago, few applications existed outside the typical Sound Blaster games. Now, with multimedia extensions built into Microsoft Windows and the growing number of associated business applications, users find that the sound board is a necessity, not a luxury. In addition to the sound board, many users employ some type of SCSI peripherals that require a host-adapter interface board. Hence, if the sound board and host-adapter board were combined, many compatibility and real-estate problems would be solved and overall cost to end users would shrink.

That's exactly what's achieved by the AME-1570/1572 card, designed by Adaptec Inc., Milpitas, Calif. *(Fig. 1)* The 1572 differs from the 1570 in that it has the hardware available to directly connect to a floppy-disk drive. The board handles all of the audio functionality and some peripheral functions using an Analog Devices DSP multimedia chip set. The chip set consists of a digital-signal processor (the 2115), a sound chip (the 1848), and a series of integrated software libraries. Also present on the board are a joystick interface, RAM, and ROM *(Fig. 2)*.

Adaptec chose Analog Devices' architecture because of its extensive software support, which adheres to such standards as Sound Blaster and Windows Sound System. In addition, this particular DSP-based architecture lends itself to future upgrades. A next-generation board should be able to handle functions like fax and other telephony jobs without replacing the existing DSP part. To upgrade the board, a task manager would be run on the digital signal processor, then the new code would be loaded through the task manager.

Most of the popular sound cards available contain some sort of simplified SCSI interface, which is employed primarily as a CD-ROM connector. But the 1570/1572 is a full-function SCSI-host adapter that's oriented toward multimedia, meaning that it contains boot support for fast SCSI-2 disks. By simplifying the integration of multimedia into PCs, applications can integrate different data types, such as audio, video, voice, images, animation, and so on. Hence, the 1570/1572 is targeting business applications and games and entertainment.



1. THE AME-1570/1572 BOARD UNITES the functionality of a sound board with a complete SCSI-2 host adapter. The board's audio section is managed by an Analog Devices DSP chip.

In addition to removing the obvious problem of requiring two slots in the PC's backplane, the AME-1570/1572 eliminates any conflicts that come with using two separate boards. In many cases, those conflicts (e.g., interrupts,

port assignments) require the aid of an experienced user or extensive technical support.

The SCSI portion of the board is similar to the company's popular 1540C host-adapter board (based on their 6360 SCSI 2 chip), yet it contains some enhancements to the BIOS. For example, many multimedia files are so large that they don't fit onto a single floppy disk. Thus, support for 20-Mbyte floppy-disk drives is built into the card's BIOS.

Also included in the BIOS is support for removable magneto-optical drives that are frequently employed in a multimedia environment. This environment is also popular in the CAE and CAD fields, where the files tend to be quite large. Because of this extensive support that's built into the BIOS, most of the integration problems experienced by users have already been solved. The BIOS alterations also let the board boot directly from the hard drive or the 20-Mbyte floppy drive.

EASY INSTALLATION

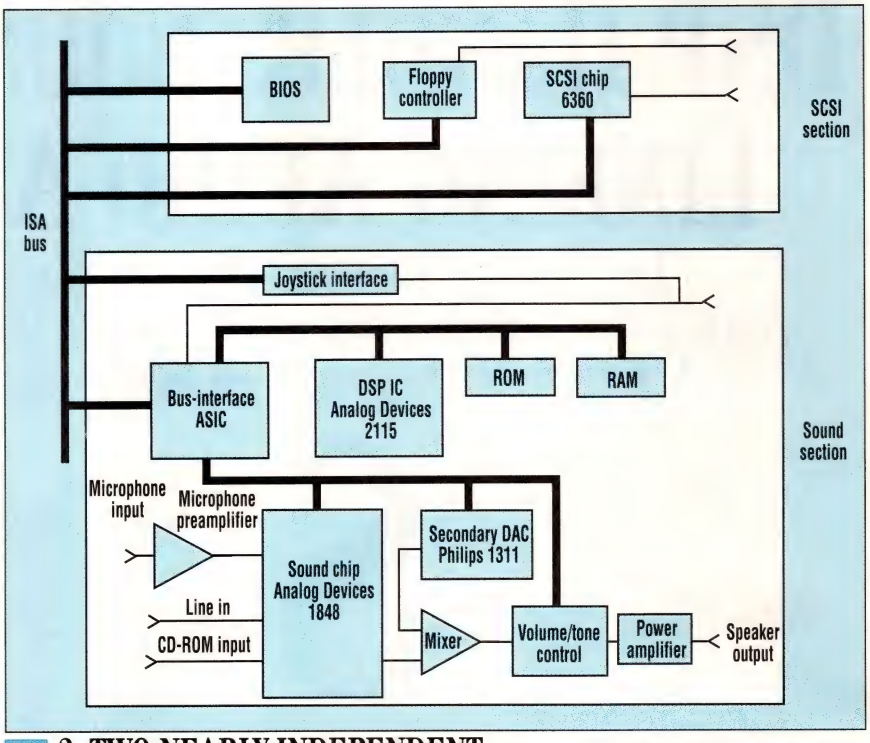
The installation process is also simplified by taking advantage of the company's EZ SCSI and EZ Audio installation software. The intelligent software "interrogates" the hardware, then loads the correct drivers and makes any necessary modifications to the system.

CD-ROM performance, which is typically characterized by a "load and play" technique, is also addressed by the 1570/1572. This means that the CD-ROM drive loads a series of images into a buffer from which they're displayed. When the buffer is empty, it gets reloaded and the process is repeated. This technique causes noticeable delays while the system is queuing up the next group of images for display.

When using XA-type CD-ROM data, rather than search for an image (such as a car) on one part of the disk and on another for the audio (such as the honking horn), the two parts are interleaved and laid down on the disk. This is called a data stream. Thus, the host-adapter board was designed to handle the streamed data from the CD-ROM.

A high-quality, adaptive-differential pulse-code modulation (ADCPM) decompression scheme takes the streamed data as it comes off the CD-ROM, then decodes the data using the DSP IC. The DSP IC next de-interleaves the audio and data, separating the audio from the image. Then, for example, the audio is sent to the speakers and the image goes to the display. The result is full-motion video that's continuously streamed from the CD-ROM.

This data separation is all handled by the DSP IC, which has complete control over the high-quality, 16-bit audio. Adaptec claims that the audio quality is higher than either Sound Blaster or the Media Vision solution. The audio scheme employed by the 1570/1572 is wave-table synthesis, wherein the board searches through a table of sounds to reproduce a particular tone.



2. TWO NEARLY INDEPENDENT subsystems—one for audio and one for SCSI—are contained on the 1570/1572 board. Each is basically a full-blown device, containing all of the functionality of two separate boards. As one board, they simplify installation and free one slot in the backplane. The 1572 has the connector to plug in a floppy-disk drive.

COMING BOARDS

Lower- and higher-performance boards are both in the works. The lower-cost board will have some of the same features, but won't require the processing power of the DSP engine. The higher-end version, which has not been completely defined yet, will take better advantage of the DSP chip to offer some increased functionality, such as advanced voice recognition. The company should announce the two new models before the end of the year. □

PRICE AND AVAILABILITY

Two versions of the AME-1570/1572 audio and SCSI host-adapter board are available, and both will go into production in April. For end users, there's a complete kit that includes the board, the EZ SCSI and EZ Audio software packages, a cable, an external connector bracket, a high-quality omni-directional microphone, and a series of diagnostic software utilities.

It also comes with the Microsoft Windows Sound System 2.0, which has its own software, including utilities for voice recognition, text to speech, and sound editing. The kit carries a list price of $399. The bare board, offered to OEMs, will sell for under $200 in large quantities. The components will also be available for integration onto a motherboard.

Adaptec Inc., 691 South Milpitas Blvd., Milpitas, CA 95035; (408) 945-8600.

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THE FIRST ICs TO REALIZE THE P1394 SERIAL-BUS STANDARD LET DESIGNERS BUILD SERIAL CONNECTIONS RUNNING AT 100 TO 400 MBITS/S.

CHIP SET SIMPLIFIES HIGH-SPEED INTERCONNECTS

DAVE BURSKY

As multimedia and other image-intensive applications become mainstream, file sizes are ballooning quite dramatically. This creates a need for faster interfaces between the peripherals and the host system. Today's parallel buses can handle short-distance high-bandwidth transfers, but the heavy cables with a dozen or more signal lines are unwieldy and prone to signal deterioration and noise. Furthermore, the wide buses require considerable back-panel space for large connectors, and as computers continue to shrink, that space comes at a premium.

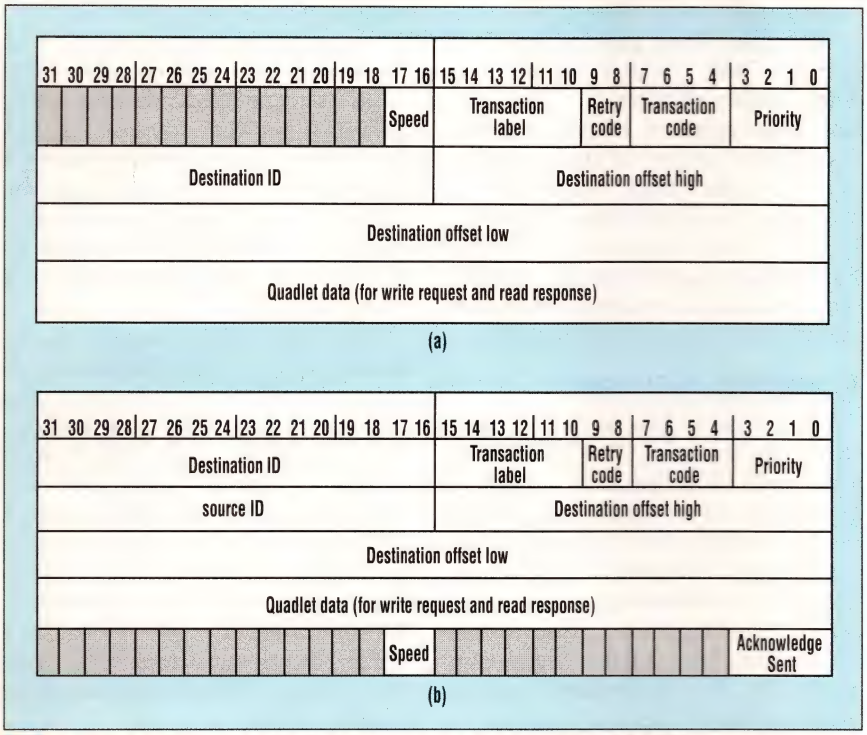
High-speed serial buses can solve many of the noise and signal distance-transmission issues when linking peripherals within a few feet of the host system. Based on the joint definition and development efforts of Apple Computer Inc., IBM Corp., Texas Instruments and other companies—part of an IEEE-supported committee—have defined a new serial interface, P1394, now proposed as an IEEE standard (Apple recently unveiled an implementation in its own systems under the trademarked name of FireWire).

The standard defines a six-wire serial bus that uses a differential interface to transmit or receive data at rates of 100, 200, or 400 Mbits/s. The bus approach falls somewhere in-between a point-to-point network and a fully-shared bus *(see "A short overview of P1394," p. 114)*. Of the three major companies involved in the development, TI has designed a moderately-priced chip set that implements just about the entire P1394 hardware interface (all the hardware for a node to become P1394-compliant). This first implementation will run at 100 Mbits/s.

The set consists of two chips: the 100-lead TSB12C01PZ link-layer controller, which will be housed in a thin, quad-sided flat package; and the TSB11C01DL, a triple-port cable transceiver/arbiter that will come in a 56-lead, small-outline, gull-wing plastic package. The link-layer controller transmits and receives correctly-formatted data packets and generates and checks a 32-bit cyclic-redundancy-check (CRC) word included as part of the packet to ensure data integrity.

Designed to handle all three P1394 data rates—100, 200, or 400 Mbit/s—the controller chip contains all of the core logic required by P1394 plus various configuration registers and I/O channel buffers. Depending on the speed it operates at, the link-layer controller's data-bus width to the physical-layer circuit varies from two bits wide for 100 Mbits/s, four bits wide for 200 Mbits/s, and increases to eight bits wide for 400 Mbits/s.

The physical-layer chip provides the interface to the cables. It combines both analog and digital circuitry to deliver, in the first version, an interface


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Speed
Transaction label
Retry code
Transaction code
Priority
Destination ID
Destination offset high
Destination offset low
Quadlet data (for write request and read response)
(a)
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Destination ID
Transaction label
Retry code
Transaction code
Priority
source ID
Destination offset high
Destination offset low
Quadlet data (for write request and read response)
Speed
Acknowledge Sent
(b)

1. TRANSMIT AND RECEIVE PACKET FORMATS for the TSB12C01 P1394 interface are somewhat similar. The transmit format uses three quadlets for the overhead information. One quadlet contains information on transmission speed, the transaction label, the retry code, a transaction code, and a priority level. A second quadlet contains a destination ID and the address of the destination offset high, while the third quadlet holds the address of the destination offset low (a). The receive format includes a destination ID in the first quadlet and a source ID in the second quadlet. At the end of the packet, a new quadlet is added (b). It incorporates the data-speed field and an acknowledge-sent field.

that can transfer data at 100 Mbits/s. However, the interface only consumes about 500 mW when powered by a 5-V supply. A lower-power 3.3-V version as well as higher-speed versions also are being developed. About 60% of the chip area in the TSB11C01DL consists of analog CMOS circuitry. The remainder of the chip contains logic circuits that implement the digital arbitration logic for the bus as well as the state machines that are needed for bus initialization.

The buffers on the link-layer controller are software-configurable FIFO registers that provide some data-rate adjustment between the host and the controller, and between the controller and the physical-layer interface. In addition, on-chip RAM—512 quadlets by 33 bits—offers ample storage to buffer packets.

There are three adjustable FIFO buffers—one each for asynchronous transmission, isochronous transmission, and general reception. Each FIFO is one quadlet wide (32 bits); the sum of all of the FIFOs can't exceed 509 quadlets. Transmit FIFOs are write-only types from the host interface, while the receive FIFO is a read-only type. When data is sent out, the transmission uses packets. However, packets can be classified as asynchronous, isochronous, block, etc.

A transmit packet consists of multiple quadlets, the first of which contains packet-control information and a number of unused or reserved bits, while the second and third quadlets contain the 64-bit, quadlet-aligned address *(Fig. 1a)*. The fourth quadlet and subsequent quadlets in the packet consist of data and are used only for write requests and read responses. The first quadlet defines the speed, the transaction label, a retry request, a transaction code, and a priority level. The 64-bit address defined in the next two quadlets is also divided into fields. The first defines a destination identifier, and the second defines the address of a quadlet in the destination node's address space.

Block transfers basically have a similar header format, as the first three 32-bit quadlets are the same. However, it's the fourth that now contains different fields—data length to define the number of bytes in the packet, and a sub-command field that tells the system what operation to perform on the data.

The receive packets also use a similar form for the control header, but the reserved bits in the first quadlet that were in the transmit packet now contain a destination ID (a 10-bit bus number and a 6-bit node number). Furthermore, in the second quadlet, the destination-ID field of the transmit packet is replaced by a source-ID field *(Fig. 1b)*. Following the three quadlets are the data words, and at the end of the transfer is a final quadlet that includes a speed field and an acknowledge sent field.

The depths of the FIFO buffers that hold the quadlets can be adjusted to optimize their size and thus system performance to suit the data types being transmitted. In applications where isochronous packets are large and asynchronous packets are small, the implementer could set the isochronous transmit FIFO and the general receive FIFO to a large size (200 quadlets each), and the asynchronous transmit FIFO and the physical response FIFO to smaller sizes (50 quadlets each).

To tie into a host system, the 32-bit interface on the TSB12C01 lets the circuit connect directly to a 32-bit microprocessor bus. Directly addressable registers on the chip that are accessed through a 32-bit data bus and an 8-line address bus allow the controller to be configured directly by the host system with just a few bus transfers. The host interface, which is interrupt-driven, minimizes host overhead by eliminating the need for the host to continually poll the controller to determine its state.

When the chip serves as a cycle master, it can support isochronous data transfers on four channels. The ability to handle multiple channels allows the chip and the system to implement multitasking so that multiple data streams can flow through the system simultaneously. Additional

features of the link-layer controller include the ability to detect lost-cycle-start messages and take action to restart the cycle.

The controller includes a cycle timer that contains a cycle counter, cycle offset timer, and cycle monitor. The cycle timer is used by nodes that support isochronous data transfers. The timer is a 32-bit cycle-timer register. Each node in the topology that supports isochronous data transfers will also have a cycle-timer register, and all use the lower 12 bits to form a modulo 3072 counter, which increments once every 40.69 ns (one period of the 24.576-MHz clock). The next 13 bits form an 8-kHz counter (clock period = 125 μs), while the highest 7 bits count seconds. The cycle monitor also is used only by nodes that support isochronous data transfers. It monitors chip activity and handles the scheduling of isochronous activity.

The physical-layer interface block on the link-layer controller services the digital transmitter and receiver sections and also requests access to the serial bus through the physical interface and transceiver chip. The interface also sends packets, receives packets, and sends out acknowledgements regarding the transmission and reception of packets. The transmitter section of the controller gets its input from either of two sources—the asynchronous transmit FIFO, or the isochronous transmit FIFO—and creates correctly-formatted serial-bus packets that will be sent out over the physical bus interface.

GAINING ACCESS

When data is present in the asynchronous transmit, the TSB12C01 first sends an arbitration request to gain access to the serial bus. Then it sends a packet. Data present in the isochronous transmit FIFO causes the chip to arbitrate for access to the serial bus during the next isochronous cycle. The transmitter block also sends out the cycle-start packets when the chip is the cycle master.

The receiver block takes data from the physical interface and determines if the incoming data packet is addressed to this node. If the packet is addressed to the node, the CRC word in the packet is checked and if valid, the header is confirmed (the read pointer is updated to the write pointer) in the general receive FIFO. For block and isochronous packets, the remainder of the packet is confirmed one quadlet at a time. A status quadlet is placed in the general receive FIFO after the packet's last quadlet is confirmed in that FIFO.

The status quadlet contains the error code for the packet. The error code is the acknowledge code that was sent for the packet. That acknowledge code tells the transaction layer whether or not the data CRC was good or bad. If the header CRC is bad, the header is aborted and the rest of the packet is ignored. When a cycle-start message arrives and is detected, it's forwarded to the cycle timer rather than being placed in the general receive FIFO just like other quadlet packets.

At the end of an isochronous cycle, the receiver inserts a cycle-mark packet in the general receive FIFO to indicate the end of the isochronous

A SHORT OVERVIEW OF P1394

The proposed P1394 standard is based on a memory-mapped-like architecture, which is basically a serial implementation of the IEEE 1212 parallel data-transfer standard. In the 1212 standard, a control and status register (CSR) provide standardized addressing, standardized transactions, and a set of well-defined control and status bits.

The protocol architecture in P1394 includes several layers that define all operations:

- A serial bus-management layer to supply the basic control functions and standard CSRs needed by the nodes on the bus.
- A transaction layer that defines the protocol used to perform the bus transactions.
- A link layer that provides a half-duplex data-transfer service (with reception confirmation) to the transaction layer.
- A physical layer to translate the logic symbols used by the link layer into the signals sent over the cable.

The bus-management layer performs the isochronous-channel assignment, error control, cycle-master arbitration, and arbitration for number/address assignment. In the transaction layer, read, write, and lock transactions which support the IEEE 1212 model are performed. Furthermore, the layer is optimized to handle 4-byte operations, but variable-length block operations also are supported. Link-layer features include isochronous transport control and flexible addressing using the 1212 protocol. The link layer is also optimized for 4-byte operations, but can also handle variable-length blocks.

P1394 systems will use a specially-designed copper cable rather than optical fiber to keep the cost as low as possible. The cable consists of two shielded twisted pairs for data, two wires for power, and an overall shield surrounding the twisted pairs and the power wires. The power wires can carry from 8 to 40 V and enough current to power a wide variety of peripherals.

At least four cable manufacturers have signed up to offer the six-wire cable, which will interconnect the computers and peripherals. Thus, just a small 6-pin connector is needed to tie the peripheral or computer to the cable. That minimizes cost and panel space. The cable topology allows for branching and daisy-chaining, with a maximum of 32, 4.5-m hops using the baseline cable. "Live" cable insertions and removals can be performed without causing any damage to the network, as a result, permitting on-line reconfiguration.

For small configurations, the standard makes it possible to have automatic protocol-timing optimization. This improves overall system performance. Each node in the system can have multiple ports, and data can be transferred between peripherals without burdening the host system. As a result, the host can concentrate on more time-critical tasks.

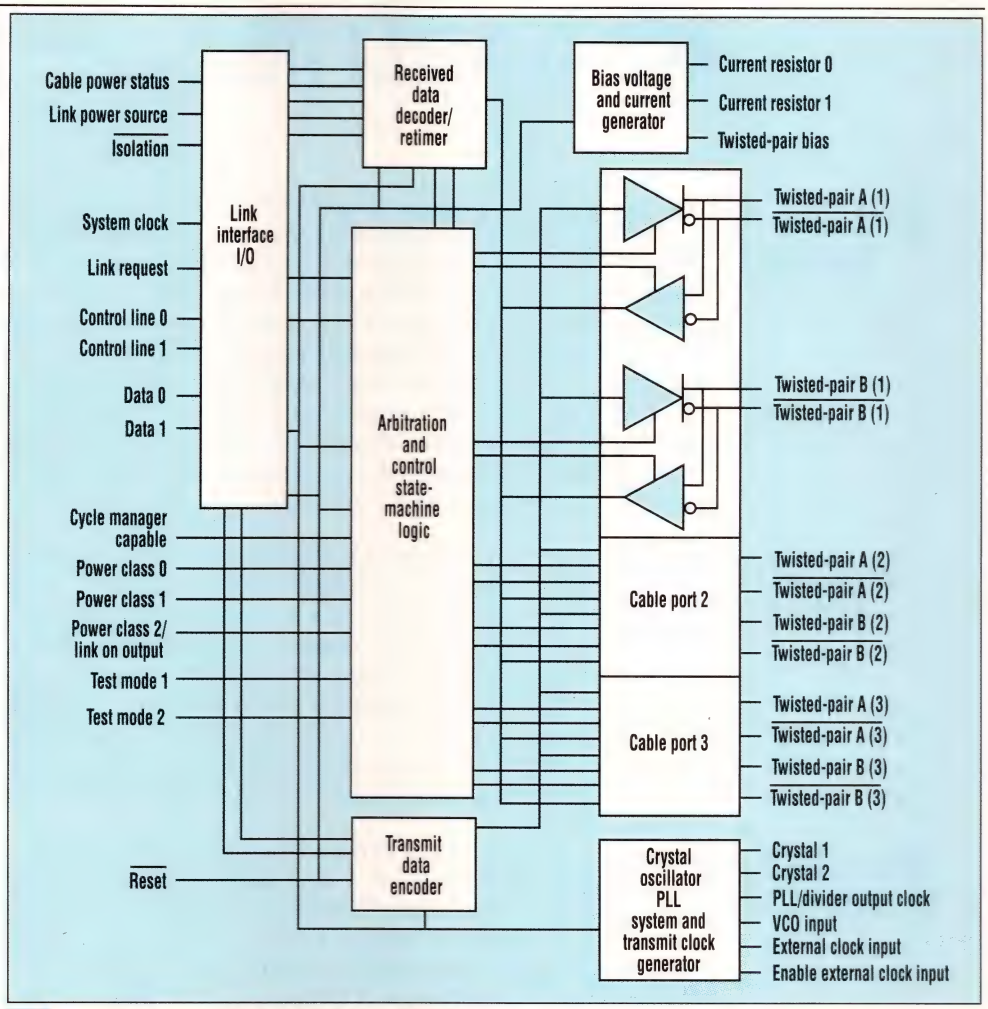
cycle. Only one confirmed and one unconfirmed packet can be placed in the general receive FIFO at any point in time. All other packets will be involved with an acknowledge code.

To tie into the physical-layer chip, the link-layer circuit uses an 8-line data bus (for 400-Mbit/s operation; 2 lines are employed for 100-Mbit/s operation), a few control lines, and a clock signal. On that interface, four operations can occur. These operations are request, status, transmit, and receive. However, except for the request operation, all other actions are initiated by the physical-layer circuit.

The physical-layer chip provides three cable ports, each providing two differential line transceivers that include circuitry to monitor the line conditions *(Fig. 2)*. Those line conditions determine connection status, initialization and arbitration, and packet reception and transmission.

An external 24.576-MHz crystal or 98.304-MHz clock source serves to set all of the timing. When using an external crystal, an on-chip phase-locked loop (PLL) generates the required 98.304-MHz reference signal; if the clock input is used, the PLL and the internal crystal oscillator are disabled. An internal divide-by-2 circuit provides a 49.152-MHz clock that controls the transmission of the outbound encoded strobe and data information. The same signal also is used as the clock for the link-layer controller. Therefore, the two chips can remain in synchronization with each other and the received data can also be resynchronized.

The physical-layer chip supports an optional electrical isolation barrier to separate itself from the link-layer controller. When pin 12, the isolation ($\overline{ISO}$) line, is tied high, the link-interface outputs behave normally. However, if tied low, the line enables internal differentiating logic and the outputs become short pulses that can be coupled through a capacitor or a transformer.



2. WITH THREE CABLE PORTS as well as port-arbitration logic, the TSB11C01DL physical-layer interface chip links twisted-pair 100-Mbit/s cables with the link-layer controller. Outputs of the port transceivers require passive termination resistors to keep the signals free from noise.

In this first implementation, data is sent over two lines from the link-layer chip to the physical-layer circuit. The data is latched internally in synchronization with the 49.152-MHz clock, by the TSB11C01DL triple-port cable transceiver/arbiter. These bits are combined serially, encoded, and transmitted at 98.304 Mbits/s as the outbound data strobe information stream. During transmission, the encoded data information as well as the encoded strobe information are sent using a differential transmission scheme on the cable pairs.

Both the twisted-pair A and B ports incorporate differential comparators to monitor the line stated during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. In addition, the twisted-pair B port monitors the incoming cable common-mode voltage to determine if a remotely-supplied 1.8-V bias voltage is present. The presence or absence of the voltage serves as an indication of cable-connection status. □

PRICE AND AVAILABILITY

The TSB11C01DL 100-Mbit/s cable transceiver chip and the TSB12C01PZ link-layer controller come in 56- and 100-lead packages, respectively, and sell for $13 and $31 each in 1000-unit lots. Samples are available immediately.

Texas Instruments Inc., 8630 LBJ Freeway, MS-8206, Dallas, TX 75265; Mike Salas, (214) 997-3426. CIRCLE 513

HOW VALUABLE?	CIRCLE
HIGHLY	533
MODERATELY	534
SLIGHTLY	535

PRODUCTS NEWSLETTER

ATM Chip Set Features Bus-Based Switching

The modular CUBIT ATM-cell switching chip and its address-header controller chip will provide engineers with easy-to-use building blocks for designing low-cost, small-to-medium-range network devices. The two chips are the first implementation of Transwitch's proprietary Cellbus technology, a cascadable bus-based architecture, which permits the switching chip to support an aggregate data rate of up to 1 Gbit/s. The ATM chip set family currently includes SAR/AAL translation functions, and chips that support a variety of physical-layer transmission technologies, including Sonet 1/3, E3, and DS3. The SAR, AAL, and transmission portions of the ATM family are available now; the switching chips will sample in the fourth quarter. To allow for early development of Cellbus-based systems, detailed specifications are available now. The Cubit will start at $91 for samples, with volume discounts as low as $51. Call Phil Richards, (203) 929-8810. *LG* CIRCLE 782

Ease Development Of C++ Applications

A development toolset for creating portable C++ applications now has a layout utility, automatic data propagation, support for portable resources, a class library, and run time type identification. XVT-Power++ from XVT Software, Boulder, Colo., has a hierarchical application framework, through which objects communicate according to standard rules. With visual layout tools, developers can quickly develop distributed applications for seven different graphical user interfaces (GUIs). The layout feature gives users an interactive WSIWYG layout of windows, dialogs, menus, and strings. XVT Power++ 2.0, bundled with the XVT Portability Toolkit, costs $1950 for Intel 486; $6300 for workstations. Call the company at (303) 443-4223. *SVT* CIRCLE 783

Mixed-Signal Simulator Blends Multiple Levels

The newest mixed-signal simulation tool from AT&T Design Automation, Murray Hill, N.J., lets users mix and match behavioral- and device-level models in one environment. A single-kernel architecture performs multilevel simulations using common databases and interfaces. Engineers can combine Spice, behavioral, VHDL, C, and gate-level models in one simulation. The simulator also provides automatic circuit partitioning—a tedious and time-consuming task if done by hand. The automatic partitioner groups tightly coupled and cross-coupled blocks, then evaluates them with individual time steps for improved accuracy. ATT's mixed-signal simulator is shipping now for HP and Sun workstations. Single-CPU licenses are $65,000. Call (908) 582-3000. *LM* CIRCLE 784

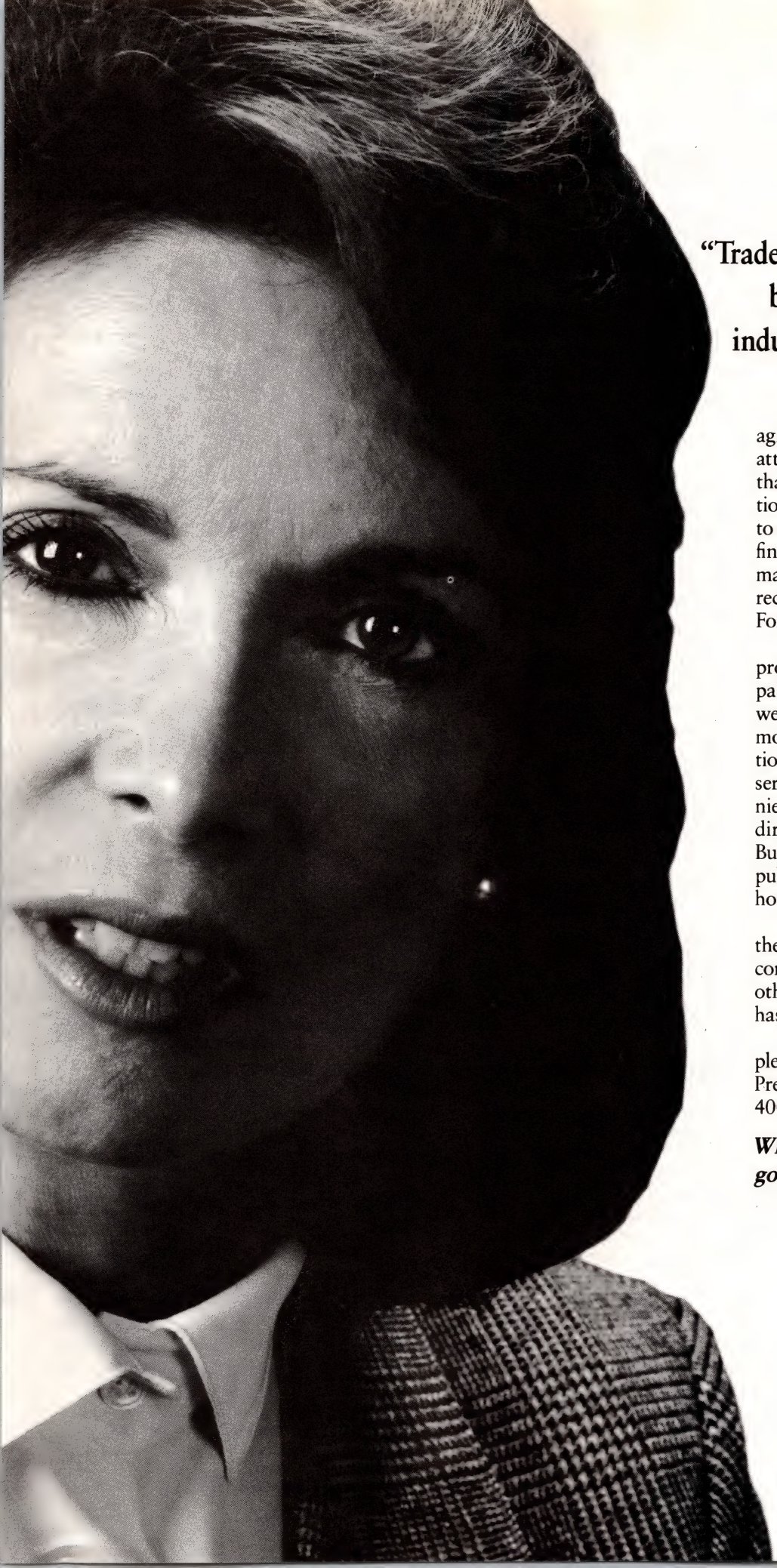
Electrometer Boasts Low Bias Current

The Model 6512 electrometer features a mere 5 fA of input bias current, less than 1 mV of burden voltage, and more than 200 TΩ input impedance. The meter, from Keithley Instruments, Cleveland, offers full autoranging over all ranges, including current from less than 2 fA to 20 mA, resistance from 100 mΩ to 200 GΩ, voltage from 10 μV to 200 V, and charges from 10 fC to 20 nC. Features include digital calibration and a 4-1/2-digit LED display that reads out in engineering units or exponential notation. A built-in 1-nA-to-100-μA decade current source can force a known constant current through unknown resistances to be measured. The $2995 meter can be controlled using front-panel pushbuttons, or through a host computer over its IEEE-488 interface. *JN* CIRCLE 785

SBus Developer's Kit Accelerates Design Times

Using the SBus/SCSI Developer's Kit, Release III, design times can be accelerated while extending product lifetimes. Based on the Solaris 2 operating environment, the kit reflects the latest hardware architectures offered by Sun Microsystems, Mountainview, Calif., including multiprocessing systems. It also contains a comprehensive reference to the Solaris 2.3 device-driver interface (DDI). Four manuals come with the kit. The first, the SBus handbook, is a guide to design considerations for Sun hardware and IEEE SBus protocol information. The second, SunOS 5.3 Writing Device Drivers, includes a diskette of sample device drivers and utilities. The other two are Writing FCode Programs, Version 2, which contains Forth language extensions, and The OpenBoot Command Reference, Version 2, which covers Revision 2 of OpenBoot. The kit is available now from either PTR Prentice Hall Publishers, or from SunExpress, for $215. Contact PTR Prentice Hall at (201) 592-2657, or SunExpress at (800) 872-4786. *RN* CIRCLE 786

Edited by Clifford Meth



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Your customers and prospects agree that trade shows are worth attending. But they also agree that specialized business publications are worth a great deal more to them. Because that's where they find more of the important information they need to know. A recent study, conducted by the Forsyth Group, proves it.

Almost 10,000 business and professional decision makers participated in the study. They were asked what sources they find most useful in providing information about the products and services they buy for their companies. Trade shows, salespeople and direct mail were all well regarded. But overall, specialized business publications clearly took top honors.

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Where business goes shopping. **ABP**

CUSTOMIZED 8-BIT MICROCONTROLLER SIMPLIFIES INTERFACES TO MAGIC BUS

DAVE BURSKY

Providing designers the first integrated solution to simplify the task of tying into the recently unveiled General Magic's Magic Bus, the M37690 microcontroller combines the bus interface with an 8-bit processor and various peripheral functions. Partnering with General Magic, designers at Mitsubishi crafted the M37690 using the processor core of its MELPS 740 microcontroller family.

In addition to the core processor and the Magic Bus interface, the MCU includes 16-kbytes of ROM; 512 bytes of RAM; three cascadable 8-bit timers; one 16-bit timer and a watchdog timer; a serial UART; a real-time clock; and 46 I/O lines (five 8-bit I/O ports and one 6-bit port). That combination of resources allows the microcontroller to provide the intelligence and functionality needed for a base docking station, a keyboard, a barcode reader, a smart telephone, or many other peripheral functions. The Magic Bus specification defines a six-line bit-serial daisy-chained bus that allows data to move at rates from 250 kbits/s to 14.7 Mbits/s. To get the high transfer rates, the data is set up as packets, which are then sent using clock-synchronous transfers. The bus has a limited loading of just six daisy-chained nodes with a maximum cable length of 0.5 meters between nodes. Peripherals that connect to the system can be "hot plugged"—plugged in or unplugged with the system running. The system software automatically updates the peripheral-mapping tables to add or remove the peripheral from the I/O address map.

The Magic Bus interface on the microcontroller has its own power supply and ground lines, so it can be powered separately from the CPU to provide the necessary signal feed through even if the peripheral is turned off. The power to keep the Magic Bus interface active is sent over two of the six wires in the serial cable. In addition to the power connections, the uplink side of the Magic Bus interface on the controller chip includes three signals—Uplink Clock, Uplink Data, and Uplink Interrupt Output. The other side of the interface also has three lines—Downlink Clock, Downlink Data, and Downlink Interrupt Input. Based on a 0.8-μm CMOS process, the microcontroller consumes just 20 mW when clocked at 5 MHz and powered by a 5-V supply. The chip, however, can also operate at 3-V, so it is directly compatible with the 3.3-V Magic Bus specification. But even at 3-V, the chip gives up nothing in performance—it can run at clock frequencies as high as 20 MHz. At that speed, many of the microcontroller's 71 instructions can execute in just 100 ns each.

Support tools for the MCU include most MELPS-family development tools—relocatable cross-assemblers, linkers, symbolic debuggers, and real-time tracers, all of which run on IBM and compatible PCs. In-circuit emulator boards, EPROMs, piggyback evaluation chips, and debugging units are also available. Hardware emulators, assemblers, and debugging tools are available from Sophia Systems, Mountain View, Calif.

Housed in a 64-lead quad-sided flat plastic package, the chip comes in a masked-ROM or one-time-programmable EPROM implementation. A fully reprogrammable UV EPROM version will be available in a windowed ceramic package. Production begins in July. Until then, an emulation MCU that only operates at a maximum clock rate of 5 MHz is available for prototyping. In lots of 25,000 to 100,000, the masked-ROM version sells for $4.70 each.

Mitsubishi Electronics America Inc., 1050 East Arques Ave., Sunnyvale, CA 94086; Ike Saeed, (408) 730-5900. **CIRCLE 800**

1.8-V OPERATION COMES TO MICROCONTROLLERS

The 68HL05 series is the latest addition to a family of low-voltage microcontrollers developed by Motorola. The new series of MCUs require just 300 μA from a 1.8-V supply and can run in systems that have bus speeds of up to 500 kHz.

The 68HL05 MCUs provides a greater than threefold power savings over 3-V versions of the same chip. The microcontrollers include seven different configurations, with varying amounts of read-only memory and random-access memory. ROM ranges from 512 bytes to 12 kbytes; RAM capacities span 36 to 176 bytes.

Each microcontroller comes with either a simple 16-bit counter/timer or a multifunction counter/timer suitable for real-time operations. In addition, there are from 10 to 28 programmable I/O lines. Three of the MCUs—the 68HCL05C4, C8, and C12—include both the SCI and SPI serial ports (SCI is a full UART-like serial interface; SPI is a simple three-wire peripheral interface). No serial port interface is provided for three other configurations, the 68HCL05J1A, K0, and P1. The last configuration, however—the 68HCL05P4—includes a SIOP serial port.

The 68HCL05C12, J1A, and K0 all come equipped with one to four high current pins along with pulldowns that can be configured with either a mask option or via software. The 68HCL05J1A and K0 also have keyboard interrupt capabilities. These processors are available in packages that come with 16 to 44 pins in either PLCC, QFP, SDIP, DIP, or SOIC formats. The 68HL05 microcontrollers start at $1.07 each in OEM quantities. All versions of the MCUs are available now. CA

Motorola Inc., CSIC Div., P.O. Box 52073, M/D 56-102, Phoenix, AZ 85072; (512) 891-2035. **CIRCLE 801**

IMPROVED DG400 SERIES GUARANTEES 3Ω *MATCHING* & 4Ω R_{ON} *FLATNESS* FOR FREE!

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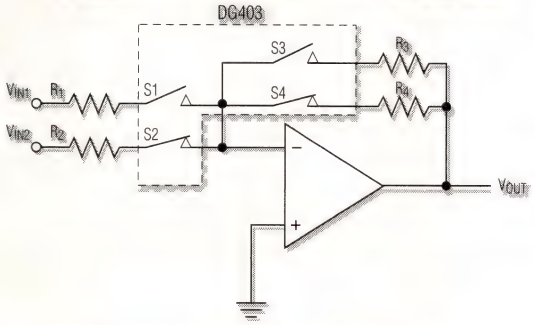
PROGRAMMABLE GAIN AMPLIFIER



Switching into a virtual ground reduces distortion caused by $r_{DS(ON)}$ variation over the analog signal range. Guaranteed $r_{DS(ON)}$ matching (typically 0.5Ω) ensures gain accuracy of <0.01% when R1 through R4 are greater than 10kΩ.

Maxim's new, improved DG400 series of switches are upgrades to industry-standard DG400 devices. These devices meet all original DG400 specifications. Their tested parameters for R_{ON} matching and flatness have never before been guaranteed. These new specifications assure lower distortion and improved linearity and accuracy for attenuators, tuned filters, sample and hold, and programmable-gain amplifiers. All switches operate over a wide supply voltage range of 10V to 30V or ±4.5V to ±20V.

ONLY MAXIM OFFERS IMPROVED PARAMETERS ON ALL DG400 FAMILY PARTS

IMPROVED PRODUCT	R_{ON} MATCH (Ω)	R_{ON} FLATNESS (Ω)	Q_j (pC)	OFF LEAKAGE at +85°C (nA)	ON LEAKAGE at +85°C (nA)
DG401/3/5	2	3	15	5	10
DG411/2/3	3	4	10	5	10
DG417/8/9	3	4	10	5	10
DG421/3/5	3	4	10	5	10
DG441/2/4/5	3	9	10	5	10

- **Guaranteed On Resistance Match Between Channels (3Ω)**
- **On Resistance Flatness (4Ω) Over Signal Range**
- **Guaranteed Low Charge Injection (as low as 10pC)**
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RESISTOR NETWORK'S SQUARE CORNERS AID INSPECTION

OEMs using visual placement-inspection equipment know the difficulties posed by components with rounded corners. Sawed-off corners can cause the machines to miss components, resulting in false reports of bad boards. Now, ROHM has developed a square-cornered version of its MNR-34 chip resistor network (MNR34K5ABJ) that provides precise visual reference points.

The square-cornered version of the MNR-34 offers the same four resistors in a 0.2-by-0.1-in. space. The resistance range for the 0.063-W/element device is 10 Ω to 1 MΩ with rated voltage of 50 V maximum.

Large solder pads and projecting electrodes present on the package offer additional benefits in assembly and application. The surface-mount solder pad promotes a strong bond between the component and the board and reduces solder paste by about 40% compared to molded networks. In addition, the projecting shape of the electrodes assures detachment of solder between adjacent electrodes, which reduces opportunities for bridging. The terminal pitch is 1.27 mm.

Chip resistor networks also provide advantages compared with single-chip resistors. They facilitate higher component densities than do single-chip resistors, which require minimum component separations of 0.5 mm. This means that the space savings of a four-pin network compared with its functional equivalent in single-chip resistors is 32%. The MNR-34 resistor network's design reduces the number of components in pc boards, resulting in lower placement costs and greater productivity.

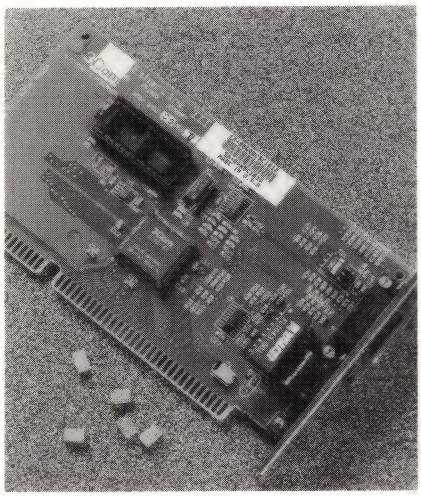
The MNR34K5ABJ chip resistor network is offered on tape and reel in 4000-piece quantities. Pricing is $50 per thousand in lots of 100,000. Delivery is in eight weeks.

ROHM Corp., 3034 Owen Dr., Antioch, TN 37013; Sherry Firebaugh, (615) 641-2020, ext. 116. CIRCLE 802

■ *DAVID MALINIAK*

RESETTABLE DEVICES PROTECT INTERFACES

New versions of the resettable, surface-mounted PolySwitch circuit-protection device are available for applications in computer interface



ports (such as SCSI, Ethernet, or keyboard or mouse ports) and peripherals (such as disk drives). For design flexibility, the PolySwitch SMD200 and SMD250 devices offer higher current-carrying capability and lower resistance than previous versions. Current ratings now range from 0.3 to 2.5 A, maximum voltage ratings run from 15 to 60 V, and resistance ratings are as low as 0.1 Ω. Unlike fuses, which are one-shot devices, the PolySwitch protectors reset themselves once the fault current is removed. Call for pricing and delivery. DM

Raychem Corp., 300 Constitution Dr., MS 530/7568, Menlo Park, CA 94025; Kathy Kelly, (800) 272-9243, ext. 6900. CIRCLE 803

MINI BRUSHLESS FANS COOL SYSTEMS DOWN

Designed for maximum performance and with ultra low voltage and wattage, the E Series mini brushless dc fans provide airflow of 0.13 meters^3/min. with a static pressure of 2.3 mm (H_2O). The 40-by-40-by-10-mm fans are available for operation from 12 V dc at 0.04 A, 5 V dc at 0.09 A, and 3.3 V dc at 0.12 A. They weigh less than 16 grams and produce low noise of less than 21 dB maximum at 1 meter. MTBF is specified at 50,000 hrs for ball-bearing construction and 20,000 hrs for sleeve bearings. Custom designs are available. Call for pricing. DM

Operating Technical Electronics Inc., 850 Greenview Dr., Grand Prairie, TX 75050; (214) 641-7089. CIRCLE 804

CUSTOM DISPLAYS SUIT MEDICAL USES

Custom-designed LCDs and LCD modules provide medical personnel with quick recognition and easy interpretation of application-specific, patient-related information. Customizing options for the displays, which also lend themselves to instrumentation, include the use of icons and symbols associated with the medical industry; combining digit and character information with icons or graphic formats; and a variety of colors. The LCDs have a wide viewing cone and numerous backlight options make them visible in all lighting conditions. Call for pricing and delivery information. DM

Standish Industries Inc., W7514 Hwy. V, Lake Mills, WI 53551; (414) 648-1000. CIRCLE 805

MICROSTEP DRIVER PROVIDES 1200 W

Designed to meet the needs of medium- to high-volume OEMs, the CMD-260 Series of bipolar, chopper microstep driver modules provides 1200 W of power in a package measuring 5 in. long by 4.4 in. wide by 0.85 in. deep. Features include microstepping, mid-range stabilization, status LEDs, full short-circuit protection, optical isolation, pluggable connectors, and DIP-switch setup. Up to 16 switch-selectable step resolutions to 50,000 steps/revolution are available, as are continuous speeds to 3000 rpm and static torques from 15 to 400 oz-in. Single-unit pricing is $450 with delivery from stock. DM

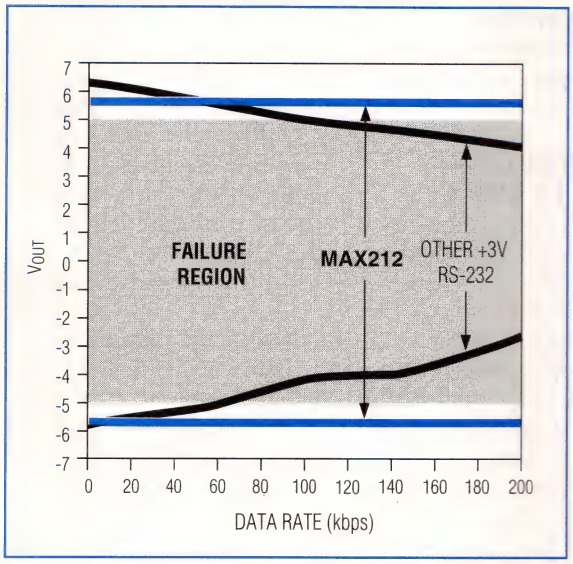
American Precision Industries Inc., Controls Div., 4401 Genesee St., Buffalo, NY 14225; (716) 631-9800. CIRCLE 806

TRUE +3V RS-232 IC REDUCES POWER 8 TIMES!

Complete Serial Port Runs at 120kbps & Drives a Mouse @ 3.0V!—GUARANTEED

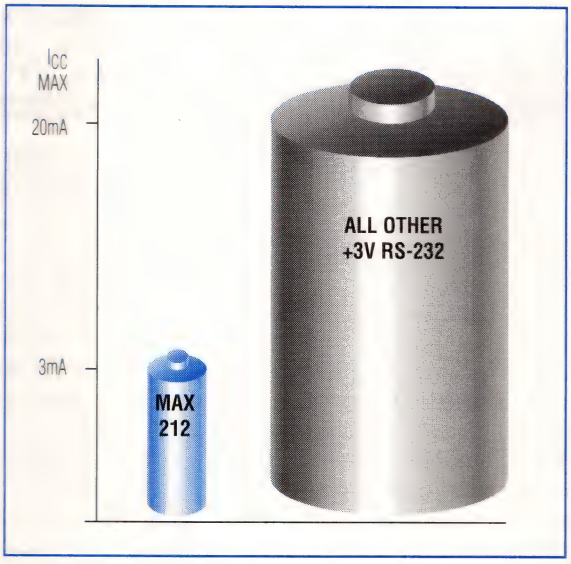
Maxim's new MAX212 has the highest data rate and the lowest power of any 3V RS-232 IC. And, the MAX212 is the only +3V RS-232 transceiver powerful enough to drive a mouse at 3.0V!

120kbps DATA RATE—GUARANTEED!



A regulated output stage guarantees RS-232 output levels are met; even at 120kbps!

REDUCE POWER 8 TIMES!



The MAX212's proprietary architecture reduces power 8 times!

Select the Low Power +3V RS-232 Transceiver for Your Design

Part	ICC (max)	Data Rate	RX Active in Shutdown	Description
MAX212	**3.0mA**	**250**	**5**	**True RS-232 From +3.0V**
MAX560	8mA	120	2	Meets Low Power EIA/TIA-562
MAX561	8mA	120	0	Pin Compatible with MAX241

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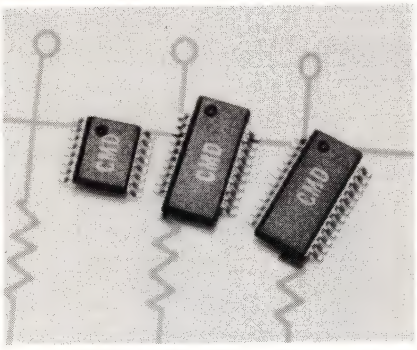
COMPLEX R-NETWORKS TERMINATE PENTIUMS

A family of highly integrated thin-film resistor networks is intended for use in line-termination applications in advanced processor-based designs. The IPEC R-Net networks specifically address the needs of sys-

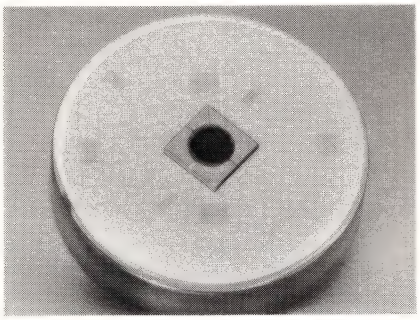


tem and board-level designers of advanced i486, Pentium, PowerPC, and other RISC-based systems. The devices also offer a replacement solution for all varieties of discrete resistors and can directly replace one or more thick-film SMT networks. Two popular configurations are available in mini-SMT package styles with standardized values for many termination, pull-up, or pull-down application requirements. In lots of 10,000, unit pricing ranges from $0.34 to $0.82, depending on type. Prototype samples are available now with production lead times running six to eight weeks. DM

California Micro Devices Corp., 215 Topaz St., Milpitas, CA 95035; (408) 263-3214. CIRCLE 807

THIN-FILM DIAPHRAGM SUITS PRESSURE TASKS

A sputtered thin-film, strain-gage pressure diaphragm is well suited for OEMs building pressure transducers as well as others with pres-



sure-measurement needs. The model P940 diaphragm is an all-stainless steel, wetted surface device with a proprietary sputtered circuit. The sputtered thin-film, full-bridge circuit provides high long-term stability and higher temperature capability. Other features include a lead-out pad design for easy soldering and rugged construction. Specifications include 0.1% full-scale-output drift per year and pressure ranges from 50 to 6000 psi. Call for pricing and delivery. DM

Strain Measurement Devices Inc., Dept. P-1, 130 Research Pkwy., Meriden, CT 06450; (203) 235-9330. CIRCLE 808

COMPACT MICROMOTOR DELIVERS UP TO 500 W

More power in less space than comparably sized motors is delivered by the GNM 80 permanent magnet dc motor. With a body diameter of 110 mm (4.3 in.) and length of 147 mm (5.8 in.), the 24-V motors produce up to 500 W at 3000 rpm. The units come with NEMA/IP 54 protection and four-pole construction. Gearing, brakes, and tachogenerators are available as optional equipment. Applications include battery-powered vehicles, material-handling systems, or any motor-driven application in which short motor length is a critical characteristic. Prices start at $340 in small quantities. DM

Micro Mo Electronics Inc., 742 2nd Ave. South, St. Petersburg, FL 33701; (813) 822-2529. CIRCLE 809

WIDEBAND MIXER COVERS 5 TO 2500 MHz

A wideband mixer that covers 5 to 2500 MHz, the model RMS-25MH, is a miniature surface-mounted device that features an all-ceramic case measuring 0.25 by 0.31 by 0.20 in. Despite its small size, the mixer delivers high LO-RF and LO-IF isolations of 32 dB typical. The component also provides especially good typical VSWR specifications of 1.60:1 (LO), 1.6:1 (RF), and 1.10:1 (IF). They exhibit flat conversion loss over the entire band. All connection pads have a solder-over-nickel barrier for improved leach resistance and excellent solderability. Featured is an all-welded internal construction that's capable of passing MIL-M-28837 shock and vibration tests. Operating and storage temperatures range from –55 to 100°C, and units are available in tape-and-reel format for high-volume production. In quantities of 10 to 49, pricing is $7.95 including a five-year guarantee. Delivery is from stock. DM

Mini-Circuits, P.O. Box 350166, Brooklyn, NY 11235-0003; (718) 934-4500. CIRCLE 829

PHOTODIODES RESPOND IN VISIBLE RANGE

A pair of silicon photodiodes, the S5493 and S5627, provide a response similar to visual sensitivity. They reject ultraviolet and infrared wavelengths without the visual-compensation filters that sometimes make silicon photodiodes unreliable in harsh environments. Typical dark currents are 20 pA for the S5493 and 10 pA for the S5627. Rise times are 10 ms and 2 ms, respectively. The surface-mountable devices have an operating-temperature range of –25 to +85°C and are housed in clear epoxy-molded packages. Applications include auto-exposure systems that provide control for strobes, copiers, and displays. Both are available for immediate delivery. Call for pricing information. DM

Hamamatsu Corp., 360 Foothill Rd., Box 6910, Bridgewater, NJ 08807-0910; (908) 231-0960. CIRCLE 830

MONOLITHIC COUPLER OFFERS WIDEBAND USE

A single-mode, wideband, monolithic 1-by-4 coupler is claimed as an industry first. The compact device meets the fiber-optic industry at its point of need with greater flexibility in installation and operation. The dual-window device provides a nominally equal coupling ratio at both 1310 and 1550 nm. The devices are used primarily in cable-television and fiber-in-the-loop applications. They conform to the latest Bellcore specifications. Couplers come in star and tree configurations from two to 32 ports and can have any split ratio for applications such as distributed-fiber networks. Call for pricing and delivery information. DM

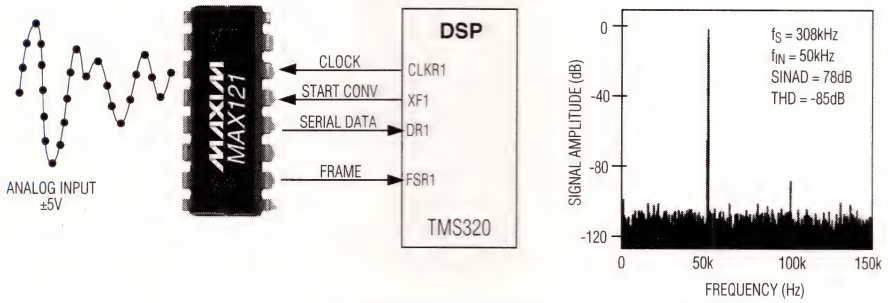
AOFR Americas Inc., 800 E. Campbell Rd., Suite 108, Richardson, TX 75081; Stuart Barr, (214) 644-1394. CIRCLE 831

UPGRADE YOUR DSP SYSTEM 6dB—FREE

14-Bit 308ksps Serial ADC for Only $12!*
Direct Interface to DSP

The new MAX121 is designed and tested specifically for DSP, and delivers 78dB SINAD, at least 6dB more than comparably priced 12-bit ADCs!

DIRECT SERIAL INTERFACE TO TMS320 AND OTHERS WITH NO GLUE LOGIC!

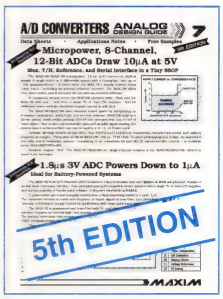


Data Sheet includes application note with source code for easy interface to your DSP processor.

- **308ksamples/sec throughput**
- **Interfaces to TMS320, ADSP2101, µPD77230, SPI, QSPI, µWire, & Others**
- **Internal Track/Hold & Reference**
- **Low Noise & Distortion: -85dB THD, 78dB SINAD**
- **1.5MHz Full-Power Bandwidth**
- **Small Package: 16-pin DIP, SOIC & SSOP!**

Evaluation Kit Speeds Design

The kit comes fully assembled, and provides a proven high-speed design and layout for fast easy evaluation of the MAX121 at sample rates to 308ksps. **Order MAX121EVKIT-DIP, $85.†**



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*1000-up recommended resale
†MAX121 EVKIT-DIP available

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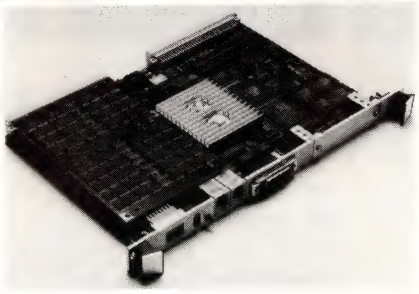
READER SERVICE 123

ALPHA-BASED SBCs SUIT REAL-TIME EMBEDDED APPLICATIONS

Embedded real-time computing is the target that two VMEbus single-board computers are aimed at. Both SBCs come from Digital Equipment Corp., and each is based on the company's Alpha family of microprocessors. One runs at 66 MHz (over 100 MIPS), the other at 166 MHz (over 200 MIPS). The two boards are part of the EBV family.

The first board is based on a 66-MHz 21068 Alpha microprocessor. It requires just one slot in the VME backplane. The second board is almost identical to the first, but it's built with a 166-MHz 21066 processor. As a result, it takes up two slots in the backplane because of the large heat sink that's required to cool the high-speed CPU.

The boards run either DEC's OSF/1 Unix operating system with real-time extensions or its DECelx real-time kernel for embedded systems. DECelx makes it possible for designers to employ a host computer to build applications for the Alpha-based target boards. The host can be running OSF/1. DECelx is based on VxWorks, a real-time operating system from Wind River Systems. DEC ported it to the Alpha hardware and added several features.



I/O is expedited using the high-speed PCI local bus. Because PCI is an open standard, peripherals can be designed by DEC, third-party developers, or even board users. There's room for one PCI module on the board. The VMEbus interface is implemented using a standard VIC64 interface chip, which conforms to the ANSI/IEEE standard. Extensions are built in to employ 64-bit data transfers. Standard I/O comes from on-board Ethernet, SCSI-2, and two serial ports.

Up to 128 Mbytes of DRAM fit on each board. The error-correcting memory can be accessed either from the CPU or the VMEbus. There's also room for 256 kbytes of external cache and 1 Mbyte of flash EPROM.

Both boards should be shipping in the next few months. Pricing details are available from DEC. The operating systems will be available when the boards ship.

***Digital Equipment Corp.**, 2 Results Way, Marlboro, MA 01752; (800) DIGITAL.* CIRCLE 810

■ *RICHARD NASS*

MULTIBUS II BASEBOARDS HOLD 486DX2 PROCESSORS

Performance can be improved by almost three times using the latest family of Multibus II-based boards from Intel Corp. The board's Modular Interface Extension (MIX) maintains software compatibility with existing boards. Current systems can be upgraded simply by replacing the base board. No redesign is necessary.

The family is based on a 32-bit Multibus II architecture. Included firmware handles the initialization process. The boards are built with microprocessors running at up to 66 MHz. Using SIMMs, the boards can hold up to 32 Mbytes of 70-ns memory.

The boards are designed so that a variety of I/O options can be plugged into using MIX-based mezzanine boards. System integrators can either design their own modules or buy them from third-party sources. Intel offers a series of modules, including controllers for asynchronous terminals, Ethernet, and wide-area networks.

Prices for the MIX baseboards run from $2495 for a 33-MHz 486SX board without memory to $3895 for a 66-MHz 486DX2 board with 8 Mbytes of DRAM.

***Intel Corp.**, P.O. Box 58119, 2200 Mission College Blvd., Santa Clara, CA 95052; (800) 438-4769.* CIRCLE 811

■ *RICHARD NASS*

VME BOARD HOLDS EIGHT DSP CHIPS

Eight DSP chips fit directly on the MZ 7772 octal VMEbus CPU board. Because they all fit on the baseboard without using mezzanine modules, the interprocessor communications occur at a higher speed than conventional boards. The board fits a 6U VME form factor and makes use of the latest tape-automated-bonding (TAB) technology to squeeze the eight TI TMS320C40 processors on to the board. Each 50-MHz processor pumps out 50 MFLOPS, supplying an aggregate performance rating of 400 MFLOPS. In addition, each processor is configured with six 20-Mbyte/s communication ports and a six-channel DMA coprocessor. The MZ 7772 is built with a VME64 master/slave interface that supports 60-Mbyte/s block transfers. Available now, prices for the MZ 7772 DSP board start at $18,700. RN

Mizar Inc., 2410 Luna Rd., Carrollton, TX 75006; (214) 247-8849. CIRCLE 812

BOARD SPEEDS MAC FILE TRANSFERS

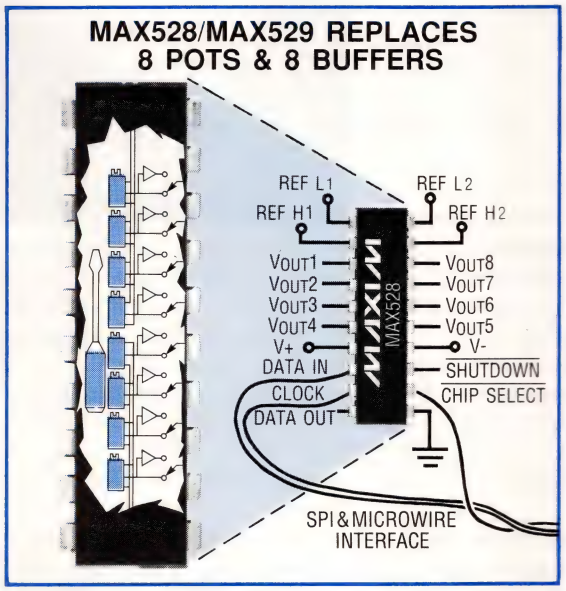
Macintosh users can take advantage of the Niwot DFT/MAC, a digital communications system that supplies high-speed file transfer over any synchronous lines. Files can be moved between locations with up to 98% utilization of selected line bandwidth, regardless of file size. The hardware-software combination includes a high-speed synchronous interface that supports most standard communications paths. Two different versions are available. One is for developers, the second is for end users. Both are available now. The developer's kit costs $1295 and the end-user model is priced at $1600 per node. RN

Niwot Networks Inc., 2200 Central Ave., Suite B, Boulder, CO 80301; (303) 444-7765. CIRCLE 813

REPLACE 8 POTS AND 8 AMPS WITH ONE IC!

Low Cost and Power Solution to Trimming System Errors

Maxim's new MAX528/MAX529 combine eight 8-bit digital-to-analog converters (DACs), output buffer amplifiers, and serial interface logic on a single chip, providing a compact digital alternative to 8 trimpot-amplifier pairs. MAX528 works with a +12V to +15V, or dual-supplies totalling up to 20V, such as +15V/-5V or -15V/+5V, to fit any analog system. And, for applications requiring single +5V and dual ±5V supplies, Maxim offers the MAX529.



REDUCE ERRORS
- Adjust System Gain & Offset Errors
- Monotonic Over Temperature

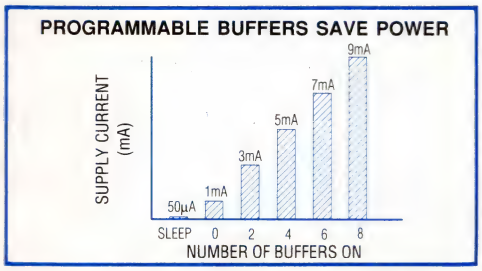
REDUCE POWER
- Supply Current: <1mA with Buffers Off
  <9mA with Buffers On
- Shutdown Mode: <50µA

REDUCE SPACE
- 3-Wire Serial Interface
- Replace 8 Pots & 8 Buffers
- Small DIP and SO Packages

REDUCE COST
- Eliminate Mechanical Adjustments
- Low Maintenance – Automate Calibration
- Cut Board Space and Component Count
- Attractive Price – MAX528 $6.90*
  – MAX529 $5.65*

Disable Buffers and Save More Power

The MAX528/MAX529 serial interface selects the DAC output mode—in full buffered mode, drive low resistance loads up to 5mA; with buffers off, drive high resistance loads directly from the DAC, achieving lowest power and highest accuracy. Buffers can be turned off in pairs, saving 2mA/pair.



MAX528/MAX529 allows connecting loads directly, or only using buffers when driving low resistances.

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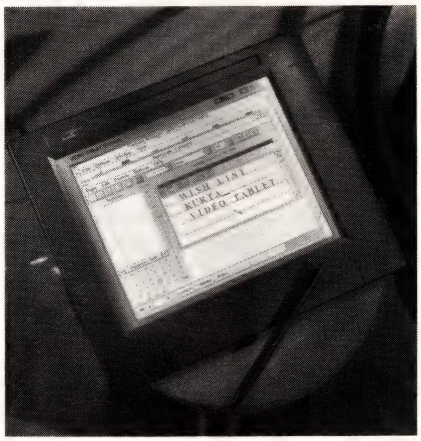
READER SERVICE 132

VGA WRITING TABLET SERVES AS A MOUSE ALTERNATIVE

A pen can be used as an alternative input device when coupled with the VideoTablet model VTS-5 writing display system, designed by Kurta Corp. In addition to being a mouse alternative, the system allows users to perform applications developed specifically for pen-based computers. This includes those applications that are compatible with Microsoft's Windows For Pen Computing.

Designed to be held and used in either a portrait or landscape orientation, the VTS-5's ergonomic display is actually a slim electronic writing tablet that's about the size of a three-ring binder, and slightly more than 0.5-in. thick. The VideoTablet is built with an STN VGA monochrome LCD that offers a resolution of 640 by 480 pixels with 64 shades of gray. The resolution of the digitizer is 1016 points/in.

The display comes with a writing pen and a VGA controller card that plugs into any ISA slot. The specialized controller card lets an external



monitor display the same data that's seen on the tablet, including the pen's cursor. Drivers are included for most of the popular pen-based operating systems. Because of the tablet's low power requirement, it can also operate with a portable PC. The VideoTablet VTS-5 writing display system, available now, is priced at $1495.

***Kurta Corp.**, 3007 East Chambers St., Phoenix, AZ 85040; (602) 276-5533.* CIRCLE 814

■ *RICHARD NASS*

PRINTER BOASTS FASTER ENGINE, IMPROVED IMAGE RENDERING

Color printing has just been improved by the Phaser 300i, a third-generation printer from Tektronix. The new device boasts an enhanced shareability, faster printing, and improved image rendering. As with previous-generation phase-change printers, the Phaser 300i is a plain-paper color printer, with a resolution of 300 dots/in., capable of supporting Adobe Postscript Level 2 software. With the implementation of Adobe IntelliSelect, which allows for automatic language sensing and switching between languages, the Phaser 300i also provides support for the HP-GL and PCL 5 languages.

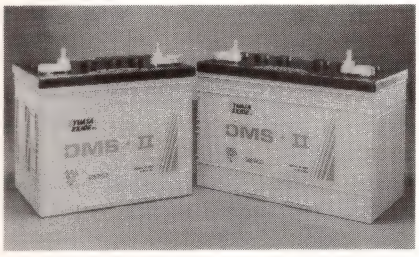
The basic printer comes with 10 Mbytes of RAM, (expandable to 22 Mbytes in increments of 4 Mbytes), and has serial, parallel, and AppleTalk ports. Consequently, it permits the printer to be shared in a workgroup. In addition, an optional internal Ethernet interface is available to support Novell Netware, Apple EtherTalk, and TCP/IP protocols. Implementation of a new print-head design, with 31 jets per primary color, along with a 24-MHz AMD 29000 RISC-based processor, provides processing power at twice the speed of previous-generation printers. Improved image rendering is achieved through the use of phase-change technology, and TekColor Finepoint, which provides extremely fine detail through high-frequency screening to optimize detail and accuracy. The Phaser 300i sells for $9995.

***Tektronix Inc.**, P.O. Box 1000, MS 63-583, Wilsonville, Ore. 97070; (503) 682-7377.* CIRCLE 815

■ *CHERYL AJLUNI*

UPS BATTERIES SUIT TELECOM NEEDS

The DMS+II line of valve-regulated lead-acid batteries is specifically designed for uninterruptible power supplies and telecommunication applications. The DMS12-250 and DMS12-300 are 12-V units rated at 250 and 300 W/cell, respectively, at



the 15-minute rate to 1.67 end volts. These batteries are specifically suited for UPS systems, where high-rate performance is critical. The DMS12-75 and DMS12-90 units are also 12-V units rated at 75- and 90-Ah capacities, respectively. These provide back-up power for various telecom applications. All use a lead-calcium grid for maximum discharge performance and absorbent glass-mat technology for optimal recombination efficiency. Call for pricing and delivery. DM

Yuasa-Exide Inc., Stationary Batteries Div., P.O. Box 14145, Reading, PA 19612-4145; Andrew Foss, (215) 378-0333. CIRCLE 816

HIGH-VOLTAGE MOSFETS BOOST BLOCKING ABILITY

Thanks to multiple rings that provide the proper field shaping toward the edge of the die, a family of power MOSFETs offers substantially enhanced voltage-blocking capability. As a result, the devices are better equipped to protect against surface charges that commonly occur at high voltages on the chips' junction termination. The new field-termination design has been introduced as an upgrade to the company's entire 400-to-600-V range of power MOSFETs. 800- and 1000-V MOSFETs using the new technology have been added as well. Designed for high-speed, high-voltage uses in power supplies, converters, and PWM motor controls, the MOSFETs are well suited for bridge circuits where diode speed and commutating safe operating areas are critical. As a pricing example, the MTY10N100E MOSFET, a 1000-V device with an $R_{DS(ON)}$ of 1.3 Ω in a TO-264 package, goes for $21 in lots up to 999. Samples and small quantities are delivered from stock. DM

Motorola Inc., MD Z-310, 5005 E. McDowell Rd., Phoenix, AZ 85018; Trudy Mystrom, (602) 244-3576. CIRCLE 817

TOROIDAL TRANSFORMERS LEAVE OUT THE BUZZ

A line of linear, toroidal power transformers is made using equipment that fully impregnates custom transformers with a low-viscosity, bake-cured varnish that produces a mechanically rigid toroid. Unlike other processes which simply dip windings in varnish, the GFS process removes air trapped under layers of insulating tape. This prevents adjacent windings from vibrating against each other under their own magnetic forces, which can cause buzzing sounds. Most designs can be made to comply with major-agency safety standards, and all are tested for turns ratios, phasing, and hi-pot withstanding. Prices range from $20 to $150 depending on size. Delivery is in 10 weeks or better. DM

GFS Manufacturing Co. Inc., 140 Crosby Rd., Dover, NH 03820-4371; (603) 742-4375. CIRCLE 818

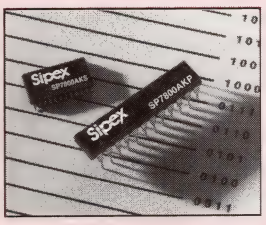
MICROWAVE TRANSISTOR DELIVERS 60-W OUTPUT

With the introduction of the LFE15600X silicon NPN microwave power transistor, Philips offers a single-ended, 60-W device suited for use in Class-AB output stages of transmitters operating in the 1.5-to-1.7-GHz band. The device's single-ended base input, plus its high power handling and diffused emitter resistors, allow transmitter powers of several hundred watts to be achieved by connecting a number of the transistors in parallel with no need for complex input-matching circuitry. Their very low 3rd-order intermodulation distortion, which is typically better than –30 dBc at 60 W peak input power, suits them for use in multicarrier transmitters such as those found in PCS base stations. The transistors are fabricated in Philips's silicon planar epitaxial technology and have a multi-cell geometry and an interdigitated emitter structure. Call for pricing and delivery information. DM

Philips Components, Discrete Products Div., 2001 W. Blue Heron Blvd., Riviera Beach, FL 33404; (800) 447-3762. CIRCLE 819

Sipex
SIGNAL PROCESSING EXCELLENCE

SP7800A Single Supply 12-Bit Sampling ADC



The new SP7800A is a SIPEX developed 3µsec, 12-Bit Successive Approximation Analog-to-Digital Converter including an Internal Reference, Clock and Sample/Hold... featuring true "Nyquist" Sampling and Single +5V Power Supply Operation.

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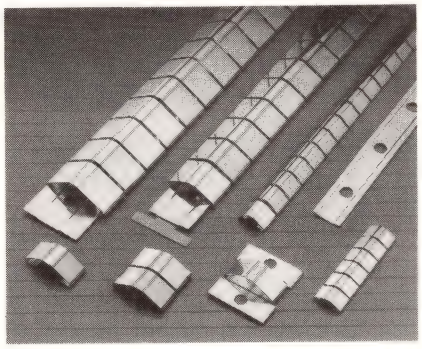
READER SERVICE 113

SNAP-ON SHIELDING KEEPS EMI/RFI AT BAY

A series of snap-on EMI/RFI shields has been upgraded with a newly redesigned mounting track that can be installed with easy-to-use plastic rivets, screws, or spot welding. The beryllium copper shielding features a "no-snag" design and provides secure mechanical fastening to ensure long life for frequently used cabinet doors and panels. Available in a wide range of plating options, the shielding is well-suited for bi-directional applications such as sliding drawers and rack-mounted assemblies. It comes in lengths up to 16 in. and in various widths. Call for pricing and delivery. DM



Tech-Etch Inc., 45 Aldrin Rd., Plymouth, MA 02360; (508) 747-0300. CIRCLE 820

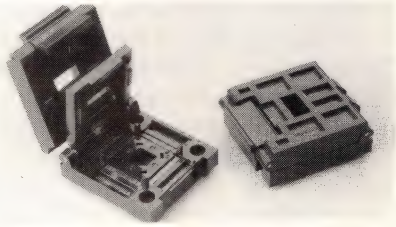
BNC T-CONNECTORS OFFER SELF TERMINATION

By integrating a surface-mounted, 50-Ω resistor into its BNC T-shaped connector, OCP Inc. has come up with a design that includes a mechanical coupling-decoupling feature with a termination function. The auto-terminating T-connectors can be used in any environment where a 50-Ω impedance is required. Other impedances can be implemented on a custom basis. When a male plug is introduced into the female jack, the connector's circuit is mechanically broken. When the male is removed, the circuit is completed and the male plug on the BNC will have a 50-Ω reflection from whichever jack is not connected, or from both. Two models are offered: the 00341 is a standard BNC T-connector with the auto-termination feature, and the 00342 also features a ground strap. Both are shipping from stock. Call for pricing information. DM

Oasis Computer Products Inc., 4757 Cardin St., San Diego, CA 92111; (619) 279-7400. CIRCLE 821

SOCKETS HANDLE QUAD FLAT PACKAGES

As an addition to its QP1 Series small-outline sockets, Nepenthe offers a 112-pin, 0.65-mm-pitch socket designed to hold a plastic quad flat pack (QFP) with a 20-by-20-mm body. The socket is suitable for high-density test and burn-in tasks. Like other QP1 models, the 112-pin QFP version features an inner-lid design that simultaneously distributes a uniform mating force along all four sides of the package. Pricing is $73.84 for small quantities. Delivery is from stock to three weeks. DM

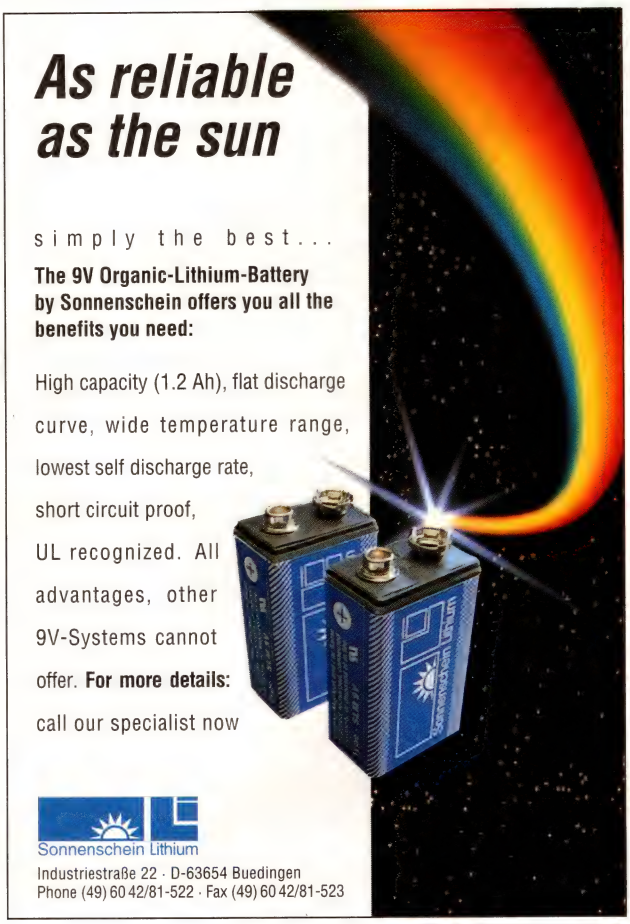


Nepenthe, 2479 E. Bayshore Rd., Suite 800, Palo Alto, CA 94303; (800) NEPENTH. CIRCLE 822

MINIATURE COAX WON'T DEGRADE SIGNALS

Low signal degradation is featured in the Acculite family of flexible, miniature coaxial cables. Made with PTFE dielectrics, the cables produce typical time delays of 1.20 ns/ft and maintain stable electrical properties at frequencies up to 100 GHz. Custom constructions are engineered to fit users' design criteria, and include multi-conductor types, miniature coaxials, balanced line, twisted-pair cables, flat ribbons, and precision miniature twisted pairs. Finished diameters of 0.05 to 0.012 in. solve routing problems. Call for pricing and delivery information. DM

Tensolite Co., a subsidiary of Carlisle Corp., 100 Tensolite Dr., St. Augustine, FL 32092-0591; (904) 829-5600. CIRCLE 823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The 9V Organic-Lithium-Battery by Sonnenschein offers you all the benefits you need:
High capacity (1.2 Ah), flat discharge curve, wide temperature range, lowest self discharge rate, short circuit proof, UL recognized. All advantages, other 9V-Systems cannot offer. For more details: call our specialist now
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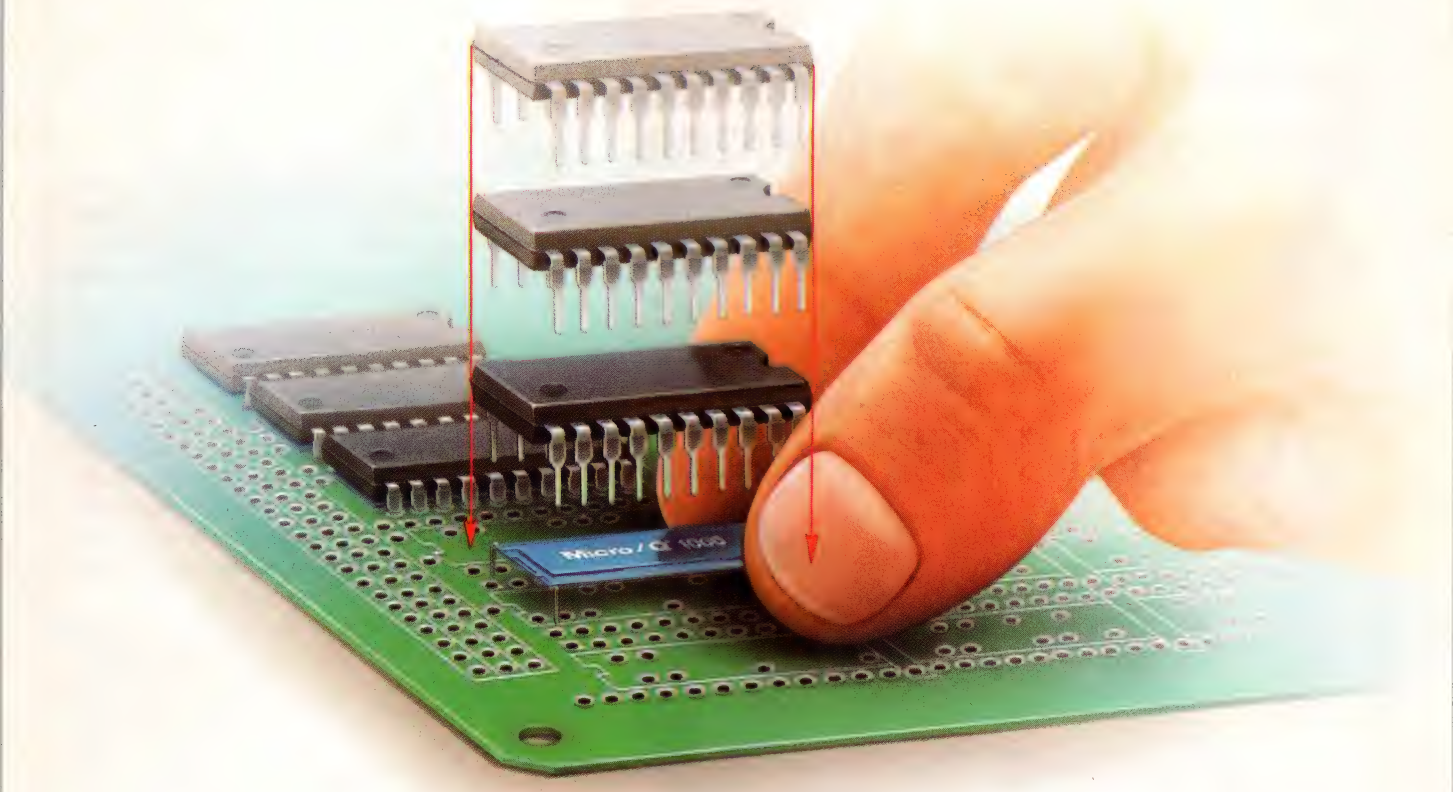
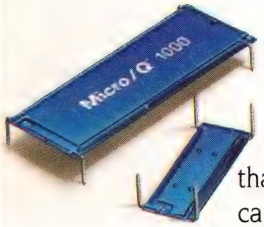
Industriestraße 22 · D-63654 Buedingen
Phone (49) 60 42/81-522 · Fax (49) 60 42/81-523

READER SERVICE 98



Noise Solutions Are At Your Fingertips.



Kill the noise and save space with MICRO/Q® 1000 decoupling capacitors.

Engineers everywhere know that when you mate CCI Micro/Q 1000 capacitors with your DIP-IC's, you'll dramatically reduce voltage noise spikes and EMI/RFI. Micro/Q 1000 is perfect for retrofitting because it is mounted under the IC and shares existing mounting holes, so you save space and improve board performance without redesign.

Low inductance means low impedance over a wide frequency range. Micro/Q 1000 is extremely effective in decoupling a wide bandwidth of frequencies with DRAMs, SRAMs, Video RAMs, EPROMs, MPUs, bus Drivers/Buffers, and various logic families. They're available in 0.3", 0.4", and 0.6" body widths with various pinouts and lengths, as well as custom pinouts to address a wide variety of specialty DIPs.

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DISTRIBUTION: Europe, Japan, Taiwan, Singapore, Hong Kong, Brazil, Australia, India • Micro/Q is a registered trademark of Circuit Components, Inc.

READER SERVICE 127

ON-SITE VXI REPAIR SERVICE USES NEW TOOL SET TO REDUCE SYSTEM DOWNTIME, COSTS

An on-site diagnostics and repair service for VXI-based test and measurement systems promises unlimited visits with either a four-hour or next-day response time, depending on the contract selected. The service is intended for owners of new or existing high-cost test systems in applications were downtime is critical and expensive. Besides offering faster diagnostics and repair, the service will allow users to stock fewer spare parts.

The service is purchased on a card-by-card basis and can cover all parts of a system—the computer, individual VXI modules, and other components. Users can easily customize or upgrade their contract service to suit their needs. Separate time-and-material repair services are available for users who do not want to place their cards under contract.

The support services will be supplied by HP's worldwide network of 3500 service engineers using the company's newly developed hardware and software tools called VXDarts (diagnostic and repair tools). VXDarts includes standards-based technology with Windows-based software written in HP VEE/PC. Diagnostic routines run on an Intel-80486 PC using standard drivers and communicating with the VXI command module through the IEEE-488.2 interface. Because VXDarts uses the open VXI standard, the tools will work with any IEEE-488.2-compatible modules, regardless of vendor.

A service engineer can connect VXDarts to the malfunctioning equipment, run the program, and interpret the results. The on-site service can be espcially beneficial for new systems, because 70% to 80% of VXI failures occur during the first year of operation.

The on-site VXI services are available now. Limited warranty conversions, Options WO1 and WO3, convert a three-year return-to-HP warranty to a one-year on-site warranty, and a one-year return-to-HP warranty to a 90-day on-site warranty for $45 per card. Options W31 and W51 provide three or five years of on-site service for $100 to $1500 per card.

***Hewlett-Packard Co.,** Directing Marketing Organization, P. O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844.* CIRCLE 824

■ *JOHN NOVELLINO*

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- Auto, R+Q, L+Q, C+D, C+R, Series and Parallel measurement modes
- 100 mV to 1.0 V test signals
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- Binning and Limits for production testing and component inspection.
- RS232 interface
- GPIB and Handler interface (optional)

SR715 **$995**

Same as SR720 except:
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- 100 Hz to 10 kHz measurement frequency

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READER SERVICE 99

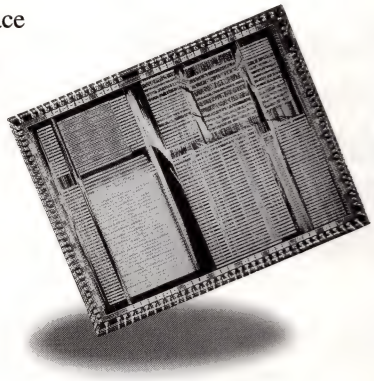
AMSC

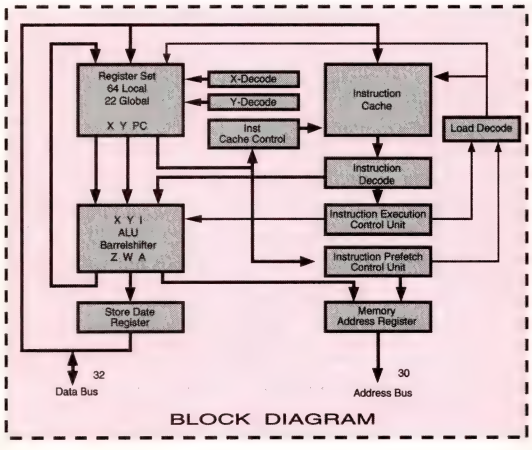
hyperstone

EFISC — Enhanced Fast Instruction Set Computer
32-bit CPU for embedded applications

GENERAL DESCRIPTION

The E1/320 hyperstone architecture combines the advantages of CISC-easy programmability, compact instruction code and low-priced additional components-with the speed of a RISC architectures. The hyperstone E1/320 has a powerful set of instructions of 16, 32 or 48bits in length. Programs for the hyperstone E1/320 require less than half of the memory space needed by most RISC processors and are even more compact than the programs of many CISC processors. Most instructions are executed in one cycle. The E1/320 is designed for various embedded control systems. As only around 85K transistors are required, the small die size makes the processor suitable for use as a microcontroller core as well.





BLOCK DIAGRAM

FEATURE

WIDE OPERATING VOLTAGE RANGE 1.8V～5.5V

LOW POWER CONSUMPTION 10mW/MHz(at 5V) 4mW/MHz(at 3.3V)

HIGH PERFORMANCE 50MIPS(with SRAM, at 50MHz)
33MIPS(with DRAM,at 33MHz)

LOW SYSTEM COST 4×1GB Memory Control (Built-in DRAM Controller).
Built-in Full-Programmable Bus-Controller. Built-in 32 bit Programmable Timer.
Use of Half-Size Cords compared with conventional RISC processor.

DEVELOPMENT ENVIRONMENT C compiler, Assembler, Source Level Debugger, Real Time Kernel, System level Debugger(PC-based), Evaluation board.

PACKAGING 144-pin Quard Flat Package(0.5mm pitch).

APPLICATIONS

Automotive equipment / Page printer / Photocopier / Factory automation equipment
Battery-driven small equipment / Mobile communication equipment
ISDN / Hand-Held information device / Facsimile / LAN / Multimedia equipment

Distributer

AMSC CO.,LTD.
1-6-5 Naka-cho, Musashino-shi, Tokyo, Japan 180

Manufacture

ALT ALPS LSI TECHNOLOGIES CORPORATION
ALPS LSI TECHNOLOGIES Co.,ltd. Yokohama, Japan.

Architecture : Hyperstone Electronics, Germany.

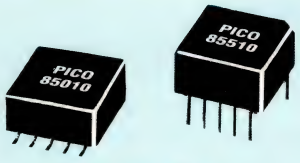
U.S.Rep. : John W. Lewis. Sumitronics, Inc. N.W. branch.
206-523-4236(TEL/FAX)
6533, 32nd ave, NE, Seattle, WA, 98115

READER SERVICE 164

PICO

Multiplex Data BUS Pulse Transformers

MIL-STD-1553



Actual Size

.4" × .4" × .2"Ht.

- Surface Mount
- Plug-In
- QPL Standards
- MIL-T-21038/27C
- MIL-STD-1553

These pulse transformers manufactured to MIL-STD-1553 COMMAND/RESPONSE MULTI-PLEX DATA BUS requirements. They also are manufactured to MIL-T-21038/27C specifications and are designed to meet MAC AIR SPECIFICATIONS A3818, A5690, A5232 and A4905.

All of these transformers exhibit superior electrical performance. Common mode rejection ratio is greater than 45dB at 1 MHz. Input impedance is greater than 3000 ohms over the band from 75 kHz to 1MHz at 1V rms. This series possesses exceptional waveform integrity: Rise time and fall time is less than 100 nanoseconds. Overshoot and ringing is less than ± 1V peak. Droop is less than 20%.

Delivery— stock to one week

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READER SERVICE 132

NEW PRODUCTS

SOFTWARE

UTILITY GIVES USERS PC SYSTEM SNAPSHOT

By inserting a disk into a PC system's A drive and turning the system on, the Computer Consultant software package runs a thorough set of system diagnostic and analysis routines. The result of the diagnostic and analysis tools is a log that details all system resources and setup parameters, easing future system configuration activities. The software will evaluate system speed, check out the amount of system memory, graphics memory, hard-disk storage space and access time, and also identify the hardware and the hardware configuration by model, manufacturer, CMOS setting and hardware settings.

A continuous speed test will be run by the software and that software will display the results in bar-graphs showing megahertz, milliseconds, transfer rates, and access rates. The Computer Consultant software can be booted from its own proprietary operating system to perform a speed test directly on the hardware, or it can be loaded under DOS to perform a speed test on the hardware and software. The program comes on both 3.5- and 5.25-in. diskettes and comes in a wallet-style case with an equipment note list pad. It has an introductory price of $49. DB

Micro 2000 Inc., 1100 E. Broadway, Ste. 301, Glendale, CA 91205; Paul Buzby, (818) 547-0125. CIRCLE 825

CALCULATION SOFTWARE HAS TWO VERSIONS

Mathcad 5.0 has trace and zoom functions for graphics, print preview, and a technical spell checker for document preparation. For advanced users, Mathcad Plus 5.0 has differential equations and advanced matrix algebra. Mathcad technical calculation software works like an electronic whiteboard, on which equations, text, and graphics can be entered for quick calculation. Users can change equations, values, and parameters, and watch Mathcad recalculate the answer with automatic unit assignment and conversion. The information can be printed as it appears onscreen with text, graphics, and equations in math notation. Both editions, which require a 386-based or higher PC running DOS 4.0 or later, run as 32-bit applications under Windows 3.1 and Windows NT compatible systems. Version 5.0 is $99.95; Plus 5.0 is $299. SVT

Mathsoft Inc., 101 Main St., Cambridge, MA 02142-1521; (617) 577-1017. CIRCLE 826

C UTILITY LIBRARY HAS 400 FUNCTIONS

Aimed at all levels of programming experience, the C Utility Library has more than 400 functions. The library includes Hyper Functions, which are subsystems of routines that function as a unit. Examples include file and directory handling, a window editor, and directory backup functions. It also has a complete set of user interface functions. User interfaces can be developed with the screen designer and code generator. The library features horizontal and vertical menus with pulldown submenus; file, list boxes, and dialog boxes; a complete set of windowing functions; shadow features; mouse support; data entry routines; fast screen handling; string manipulation; execution of DOS commands and batch files; time and date manipulations; and complete source code. Version 5.0 goes for $249. SVT

Lifeboat Publishing, 1163 Shrewsbury Ave., Shrewsbury, NJ 07702; (800) 447-1955 or (908) 389-0037. CIRCLE 828

ENVIRONMENT PORTS WINDOWS APPS TO UNIX

Chameleon technology for porting software from Windows to Unix environments forms the core of Software Pundits migration services. Chameleon is a virtual Windows software development environment for Unix. Using Chameleon, a Windows application is compiled on a Unix platform and linked to the Chameleon libraries rather than the Windows Software Development Kit. The result is a Unix-based application, identical in look, feel, and functions to the original Windows app. Contact the company for pricing.SVT

Software Pundits Inc. 25 Burlington Mall Rd., Burlington, MA 01803; (619) 229-6655; fax -6660. CIRCLE 827

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City trees add the soft touch of nature to our busy lives. They cool our cities, fight pollution, conserve energy, give wildlife a home, and make our neighborhoods more liveable.

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You can make a difference — by planting and caring for trees in your yard and in your neighborhood, and by encouraging your city government's community forestry program.

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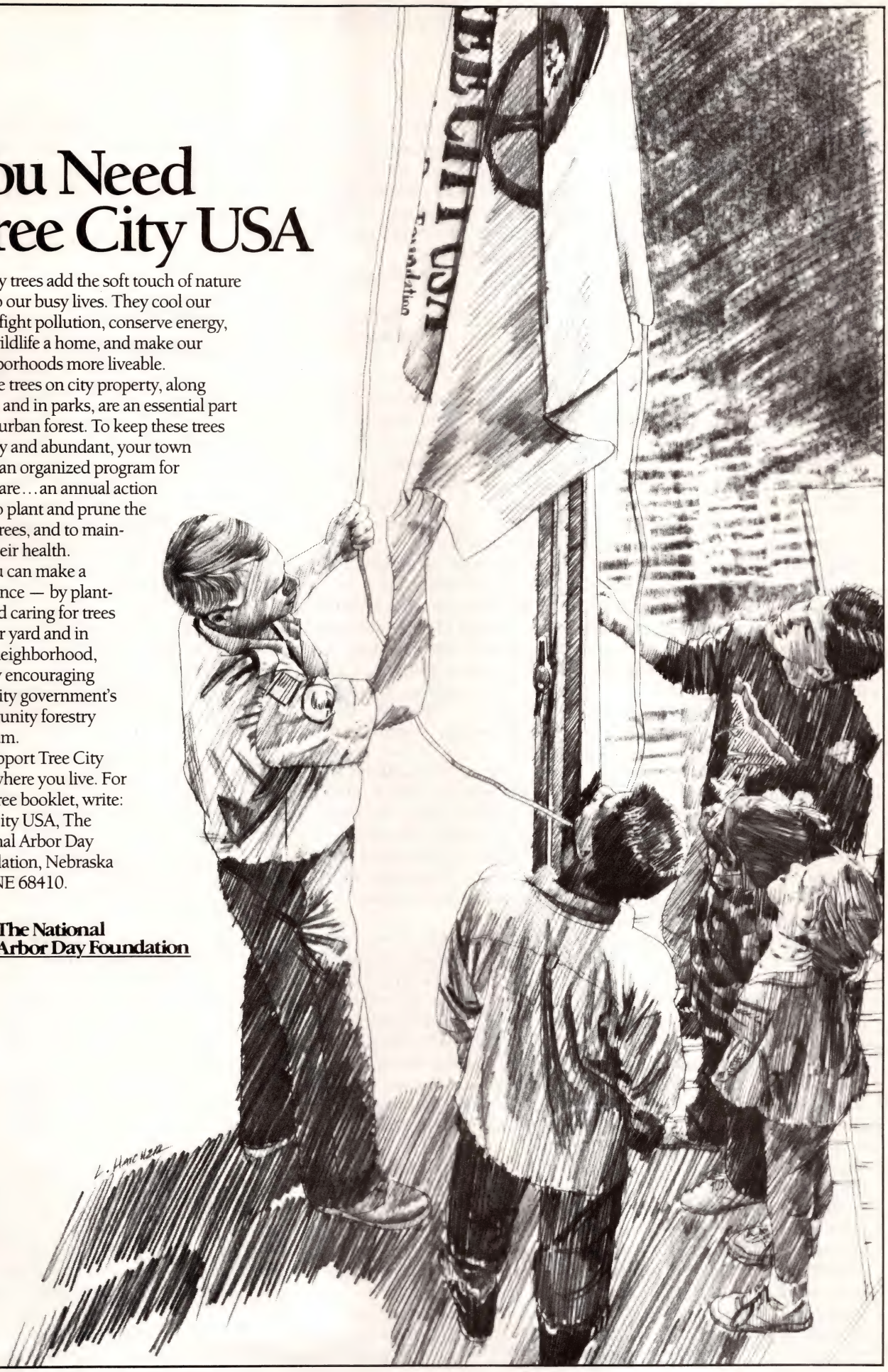
The National Arbor Day Foundation



RADIOTRON HANDBOOK: STILL VALUABLE

I, along with many of your readers, enjoy *Electronic Design's* 40 Years Ago column. The picture and accompanying editorial comments about the *Radiotron Designer's Handbook* in the Nov. 11, 1993 issue caught my attention, and I must add a few tidbits. You suspected "it didn't have the lifetime it deserved because of the industry's subsequent shift to transistors." On the contrary, as far as books on electrical engineering go, it had a substantial lifetime.

The book reviewed in your Nov. 1953 issue was the 4th edition (as mentioned). The 1st edition appeared in 1934, with subsequent editions in 1935, 1940, and 1952. I acquired mine in 1969 right after I got out of college, and it was reproduced by RCA Electronic Components in May, 1968. That spans 35 years and certainly qualifies as a substantial lifetime!

I purchased my copy because I was in the avionics end of the airline business and much of the radio equipment we used in the late 1960s was vacuum-tube-based. I designed and built test fixtures and equipment, and found the handbook quite helpful.

For the most part, there was no question the transistorized sets we had were infinitely more reliable, more accurate, and required less maintenance than their tube equivalents. However, we were stuck with the tube sets. Looking back, though, they were relatively easy to troubleshoot and certainly easier to understand at the time.

Perhaps, the reason the *Radiotron Designer's Handbook* lasted well into the 1960s is that it not only talked about tubes, but also about electronic circuits of all kinds. Subjects included the effect of feedback on phase shift, how to wind coils, a thorough explanation of the decibel, and lots of interesting audio and RF information. And where else can you find a simple, but very practical, statement such as: "A change in level of 1 dB is barely perceptible to the ear, while an increase of 2 dB is only a slightly apparent increment." I still refer to my handbook, especially when I want to know something practical and not something written by an academic who never built anything in the real world.

WHITHAM D. REEVE, P.E.
PRESIDENT
REEVE ENGINEERS
ANCHORAGE, ALASKA

Editor's note: First of all, thanks to Mr. Reeve for setting us straight on the lifetime of this excellent handbook. I myself would like to share a bizarre occurrence in relation to the book, one of the biggest coincidences I have ever been involved in.

One reason I selected this item for the 40 Years Ago column was that I owned a copy of the book and had always been impressed with its comprehensiveness and practical engineering content. I purchased my copy during my senior year (1954) at Newark College of Engineering, Newark, N.J., and held on to it for many years thereafter. I know that I still had it in the mid-70s, which, at my age, is only yesterday. In fact, when preparing the item for print, I went home fully believing I still had it. But when I searched through my basement book cache, I couldn't find it.

Last month, I received a note from Craig Merz, an engineer with ITI Manufacturing, Califon, N.J., and an Ideas for Design author (Jan. 24, "SCR-Optocoupler First-Out Detector"). After thanking us for publishing the Idea for Design, he went on to say, "Thought you might like to see the enclosed. Recently I borrowed a friend's copy of the 1952 'RCA Radiotron Designer's Handbook.' I wondered if the book might have belonged to you at one time."

The enclosure was a copy of the inside cover page. On it, in my own handwriting, were my name and a date: 1-5-54.

After convincing myself I had not entered the Twilight Zone, I called Craig and he told me that his friend bought the book at a local used book store. I have no memory of how it escaped my possession.

Steve Scrupski
Editor-in-Chief

ACRONYMS OR ABBREVONYMS?

Not to be a Grumpy Old Man or nitpicker, but regarding the Reader's Comments section in Jan. 10, 1994 issue: I disagree with those collecting stats and such on acronyms. The word "acronym" is thrown around so freely these days, I don't believe most users of this word know or have even thought about what it really means.

First, what is an acronym? I always thought an acronym was a WORD (or something WORD-like) made from the first letters of a bunch of other words. So, if you're merely pronouncing the letters of the "acronym," then it's really not one.

So, while "laser," "radar," "RAM," "ASIC," "RAID," "SPARC," and "RISC" are good examples of acronyms, I don't believe "ACS," "DMS," "PC," "EMS," "PCMCIA," "FDDI," "MCM," "PCI," "DSP," etc., are acronyms. These are simply abbreviations. Going by this, their statistics their statistics would be thrown off significantly.

But, there are some terms that are acronym-like. These don't look like words, but they're pronounced like words ... maybe we ought to call them "abbrevonyms" or something. For example, SCSI (skuh-zee) falls into this category. It looks like an abbreviation but is pronounced like a word. And, even though they don't look like any English words I've ever seen, I guess "EISA" (ee-suh) and "ISA" (eye-suh) are closer to being acronyms since most people pronounce them this way. That may not be very logical, but then again neither is the English language.

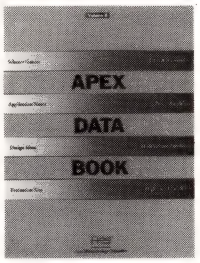
MIKE PETERS
APPLICATIONS ENGINEER
MOTOROLA INC.

SWITCH CATALOG REFLECTS USER INPUT

A 110-page catalog titled "Switching With the Times" contains product descriptions, technical information, package dimensions, and photos for the complete product line from E-Switch, Minneapolis, MN. Included are pushbutton, toggle, rocker, slide, tactile, rotary, and power switches. Many designs are original and stem directly from customer requests, while others are retrofits of existing products to provide a readily available and reliable second source. DM

CIRCLE 920

AMPLIFIER CATALOG HITS 6TH EDITION



The sixth edition of the full-line data book from Apex Microtechnology, Tucson, Ariz., covers the company's dc-dc converters, power amplifiers, high-voltage amplifiers, and high-speed amplifiers. An expanded application-notes section provides designers with technical assistance in power-amp circuits. The 366-page volume includes enhanced selector guides as well as a complete library of product data sheets. An added feature, the Simplify Your Circuit Design guide, helps designers who may be unfamiliar with hybrid and monolithic power amps to evaluate the potential benefits of using these products in their applications. DM

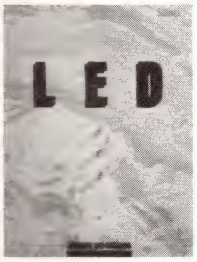
CIRCLE 921

HANDBOOK OFFERS DATA ON TEST SOCKETS

The *High-Performance Test Socket Handbook* is a guide for specifying sockets for high-performance testing applications. It contains full test-socket characterization data from an independent laboratory. Using the laboratory, the handbook's publisher, Johnstech International, Minneapolis, Minn., developed models to evaluate the usable bandwidth and other performance specifications of test sockets. The company also extracted three-dimensional Spice models for use in simulation programs to predict behavior of the socket, the system interface, the test system pin electronics, and the input and output of the device under test. Other topics in the free handbook include socket structure and contacts, applications, and mechanical performance. JN

CIRCLE 922

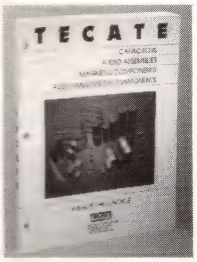
100-PAGE LED BOOK GIVES APPLICATION HELP



With over 100 pages of useful information on an extensive LED product line, a catalog from II Stanley Co. Inc., Irvine, Calif., features special material intended to assist designers and component buyers in selecting the right LED for their application. Included are a spatial distribution graph for all products and an applications section identifying where LEDs can be used. Potential uses such as office automation, audio-visual equipment, communications, automotive, and indoor or outdoor signboards are covered. DM

CIRCLE 923

CAPACITORS FILL FULL-LINE CATALOG



A full range of products including electrolytic, tantalum, and film capacitors is described in a 194-page full-line catalog from Tecate Industries Inc., El Cajon, Calif. The volume is designed for easy reference and provides specifiying and ordering information on the company' standard products as well as details of its custom capabilities. Product profiles include photos, lists of features, electrical-specification charts, application notes, and dimensional diagrams. DM

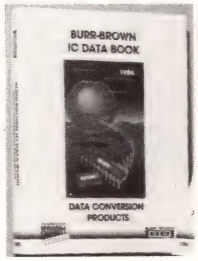
CIRCLE 924

CATALOG LISTS PC-BASED DEVELOPMENT TEST TOOLS

A 36-page, two-color catalog describes a broad range of PC-based development test instruments from the recently formed Instrument Products Div. of Emulation Technology Inc., Santa Clara, Calif. Included are in-circuit emulators, simulators, programmers, and logic analyzers, as well as related software and accessories. A solutions section discusses potential problems in project development and how the listed tools can solve those problems. Also in this section is a set of recommended PC configurations for each product, listing requirements such as memory and speed. JN

CIRCLE 925

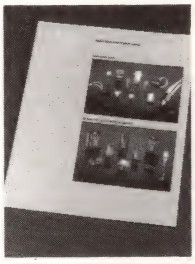
TWO IC DATA BOOKS GIVE APPLICATION TIPS



Two IC data books from Burr-Brown, Tucson, Ariz., offer complete product descriptions, application tips, graphs, specs, and ordering information. The 1100-page Linear Products book includes more than 30 new linear devices. Products include op amps, instrumentation amps, isolation products, power op amps, and more. The 950-page Data-Conversion Products book covers over 25 new devices including d-a and a-d converters, data-acquisition components, and sample-hold amps. DM

CIRCLE 926

HIGH-VOLTAGE RELAYS EXPLAINED IN GUIDE



Beginning with a simple introduction to high-voltage relays and contactors, a 75-page application and product guide from Kilovac Corp., Santa Barbara, Calif., serves as a complete reference to these device types. It explains in common language the physics of vacuum- and gas-filled relays, defines relay and contactor terms, and shows, with cutaway diagrams, typical high-voltage-relay designs. Application sections outline criteria for relay selection. Special sections include RF deratings, capacitive discharge loads, power-switching loads, and high-insulation-resistance relays. New products include 270-V-dc relays and contactors (the AP5 and AP10 Series) as well as the AP90 and AP350 Series. DM

CIRCLE 927

CATALOG/LITERATURE REVIEW

EXTRUDED HEAT SINKS

New 64-page catalog contains world's largest selection of aluminum heat sink extrusion profiles. Shows 1300 most popular shapes—all tooled. From simple bars to complex forms and hollow sections. Call 603-528-3400

CIRCLE 171

AAVID ENGINEERING, INC.

Design Tools with Power

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CIRCLE 172

ACCEL TECHNOLOGIES, INC.

Signal Integrity & EMI/EMC

Maxwell SI Eminence offers a unique, integrated solution to the whole spectrum of high speed design issues from signal delays to EMI/EMC. Characterize fullwave and radiative effects to analyze complex electronic designs.

CIRCLE 173

ANSOFT CORPORATION

DSP and I/0 Boards/Systems

New 1994 catalog of digital signal processing boards, systems and software plus a full range of analog and digital I/O for VME, Sbus and PC/AT. Systems range from single DSPs to large-scale parallel processor solutions.

CIRCLE 174

ARIEL CORP.

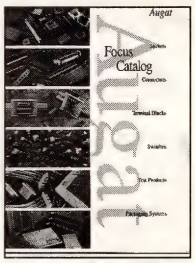
Astec's new catalog features low power supplies with high efficiency, high power supplies with PFC, distributed power modules and PC supplies meeting new EPA standards call power fax for datasheets by fax 619-439-4266.

CIRCLE 175

ASTEC STANDARD POWER

Sockets, Switches And More

New Augat 96 Pg Focus Catalog provides one-stop shopping for IC sockets, Connectors, Switches, Terminal Blocks, Test Probes, W/W Panels and Back-Planes From a Certified ISO 9000 Vendor Key Specs Included All Products in Stock.

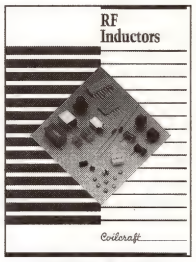


CIRCLE 176

AUGUT IPD

RF INDUCTORS

Coilcraft is offering a new RF inductors catalog showing their range of products for the RF engineer. It includes detailed specs on Coilcraft's surface mount inductors, tuneable and fixed inductors, wideband RF transformers, and L/C filter networks. Also featured is a range of designer's kits filled with sample parts to simplify prototyping.



CIRCLE 177

COILCRAFT

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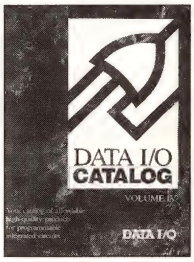
The Data I/O catalog makes our affordable tools easy to order. Phone, Fax, or mail in your order, and we'll deliver great values on high-quality design software and device Programmers. Call today for your FREE catalog.



CIRCLE 178

DATA I/O CORPORATION

Davies Molding Catalog

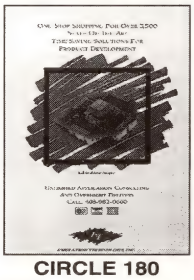
Features Attractive Top of The Line Handles Davies Molding Company, Carol Stream, Illinois is introducing an attractive and comprehensive new 56 page Handle catalog. Catalog #100 introduces unique top of the line Handles for machine tool, medical, electrical and transportation equipment applications. For a copy of Catalog #100 use the circle number to the right.

CIRCLE 179

DAVIES MOLDING CO.

VLSI/SMT SOLUTIONS CATALOG

Free '94 catalog. Over 3500 devices; 120 "off-the-shelf" items available for overnight delivery. Unlimited application consulting. Ask about our custom designs. Leading edge technology —over 500 PQFP Solutions. Time Saving Solutions.

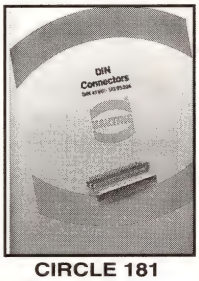


CIRCLE 180

EMULATION TECHNOLOGY

DIN CONNECTORS

Colorful brochure provides detailed information and specifications on HARTING's Gds A standard DIN 41612 printed circuit board connectors. ISO 9001 certified. Mounted & fixed to the PC board in single procedure. Wide range with many styles of shell housings.



CIRCLE 181

HARTING ELECTRONIK, INC.

SHIELDING CATALOG

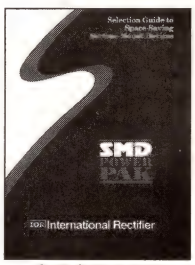
28-Pg Publication details instrument specialties BECU shielding and grounding products. Also included is information on metals compatibility, testing, engineering kits, platinting engineered stampings and assemblies and ordering.

CIRCLE 182

INSTRUMENT SPECIALTIES

Power SMDs Selection Guide

Some 250 space-saving surface mount devices covering both N and P channel power MOSFETS, Schottky diodes, IGBTs, and MOS Gate Drivers are all featured in this SMD Product Selection Guide from International Rectifier, El Sequndo, CA.

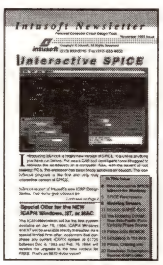


CIRCLE 183

INTERNATIONAL RECTIFIER

Spice Application Notes

The Intusoft Newsletter is a FREE publication that discusses the SPICE circuit simulation program. It contains technical articles on simulation and modeling, as well as an introduction to the NEW Interactive version of IsSpice.

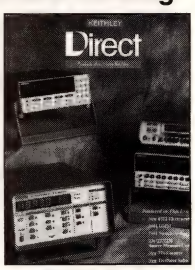


CIRCLE 184

INTUSOFT

New Keithley-Direct Catalog

Keithley Instruments is offering its new direct marketing catalog of selected test instruments and accessories. Many of the company's DMMs, switches, source-measure units and accessories are included. One of the featured products in this issue is a new electrometer. Call 1-800-552-1115 for your free copy.



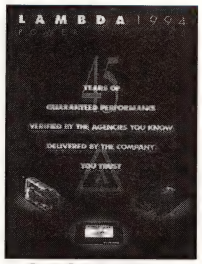
CIRCLE 185

KEITHLEY INSTRUMENTS, INC.

CATALOG/LITERATURE REVIEW

POWER SUPPLIES

A new 168 page full line catalog is available on request from Lambda Electronics Inc., N.Y.. It contains detailed information and prices on over 1000 standard power supplies, systems and accessories including 200 new products.

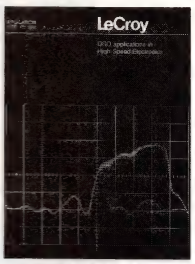


CIRCLE 186

LAMBDA ELECTRONICS INC.

DSO'S in High-Speed Electronics

A new technical note from LeCroy, intended for design engineers. Addresses problems sych as making measurements the presence of noise, cross-channel timing, crosstalk, microprocessor crashes and metastability.Call 1-800-4LeCroy Contact: Dr. Michael Lauterbach



CIRCLE 187

LeCROY

Device Programming Tools

The Newest Advances are presented in over 20 pages, illustrating the widest selection of development and production tools, PLO/FPGA Design software, UV erasers, and Prom/PLD Programmers from the leading manufacturer.

CIRCLE 188

LOGICAL DEVICES, INC.

BATTERY HOLDERS

Featured products: SMT button cell holders, battery snaps, case hardware, computer clock back-up holders, multi-cell holders with covers, auto cigarette lighter plugs. For computers, alarms, controls, instruments, toys, appliances, etc.

CIRCLE 189

MEMORY PROTECTION DEVICES

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MICROSIM CORPORATION

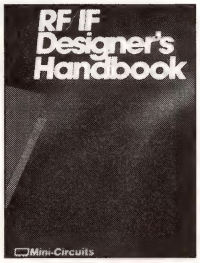
INDUCTOR CATALOG

J.W. Miller, Gardena, CA 44-page catalog and coil selector guide covers fixed & adjustable RF coils, toroids, high-current filter chokes, molded & conformal coated chokes, and surface mounted inductors...Values from .01 uH-500,000 uH.

CIRCLE 191

J.W. MILLER

Now... the most informative and comprehensiv reference manual for RF/IF signal-processing components! Mini-Circuits new 740-pg Handbook is loaded with practical articles, answers to most-frequently asked questions definitic.ıs of terms convenient selection guides, and handy conversion charts.



CIRCLE 192

MINI-CIRCUITS

Kepco 1KW Power Supplies

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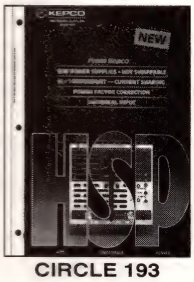
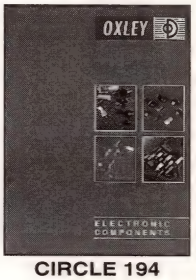


CIRCLE 193

KEPCO, INC.

ELECTRONIC COMPONENTS

1994 Catalog contains technical info on our full range of components which include: EMI/TVS Filters, Planar Arrays, Trimmer Capacitors, Led Indicators NVG Displays, Elapsed Time Indicators, Test Points for pcbs, fiber optics.



CIRCLE 194

OXLEY INC.

Embedded PC Catalog

Octagon System's, Westminster, CO, 112-page catalog displays their Micro PC® family. The Micro PC line is designed for apps. where small size wide temperature range, and rugged packaging are critical. ISO 9001 certified.

CIRCLE 195

OCTAGON SYSTEMS

Power-one Power Supplies

Power-one Reference Guide has over 200 switch-mode and linear AC to DC Power supplies, available direct or through distributors, model outputs range from 2V to 250V, up to 2000 watts, single and multiple outputs.

CIRCLE 196

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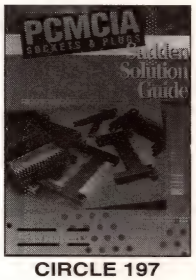
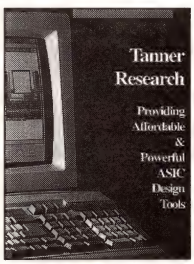


CIRCLE 197

SAMTEC, INC.

ASIC Design Software

Tanner Research, Pasadena, Calif., has a new brochure with detailed information on its complete line of affordable CAE/CAD software for ASIC design and layout. A free demo disk and price list are included.



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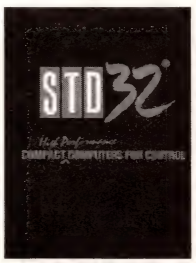
CIRCLE 199

Z-World Engineering

Small Industrial Computers

Brochure reviews STD 32, an 8-, 16-, and 32-bit industrial computer standard combining PC functionality and a compact format. A short form spec and list of manufacturers are included.



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	90	358	476	608		90	448	597	747		90	980	1305	1632
	120	385	519	649		120	486	649	812		120	1044	1420	1774

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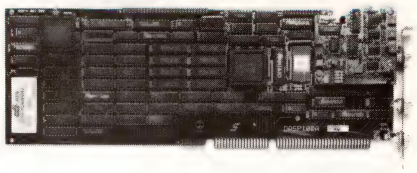

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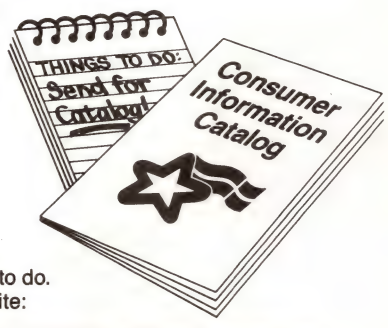

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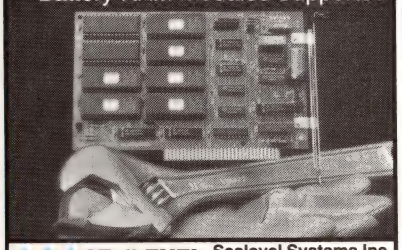

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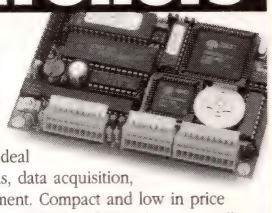

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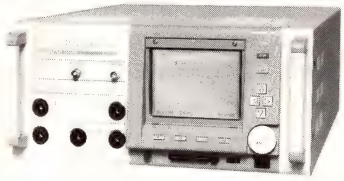

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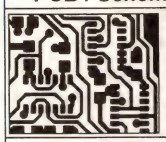

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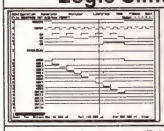

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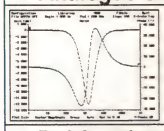

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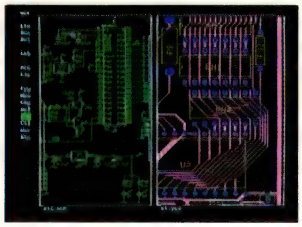

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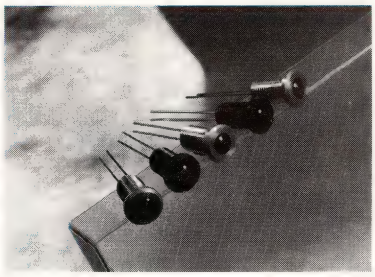

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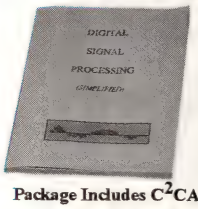

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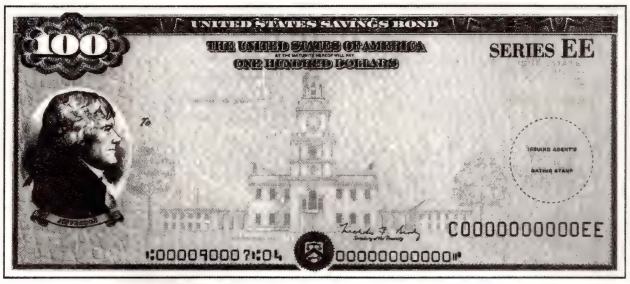

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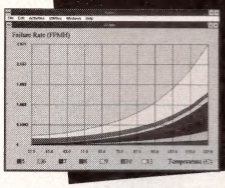

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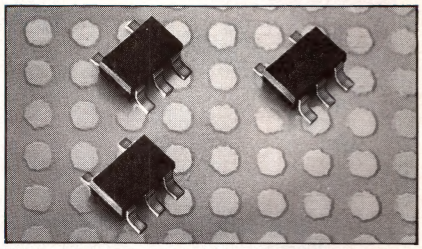

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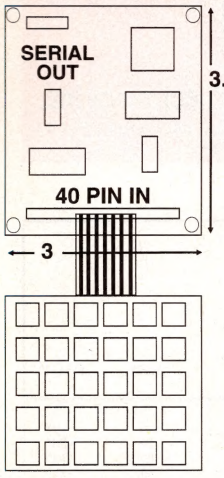

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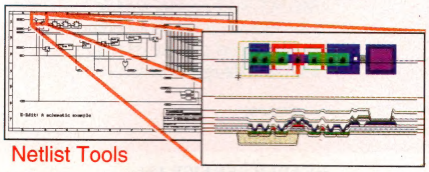

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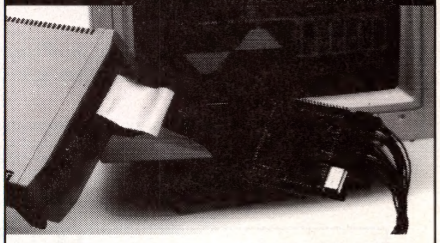

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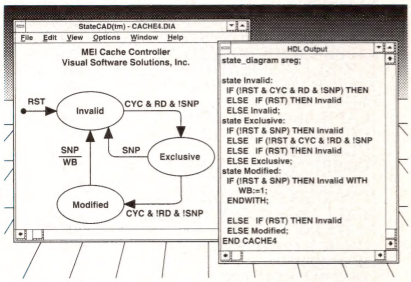

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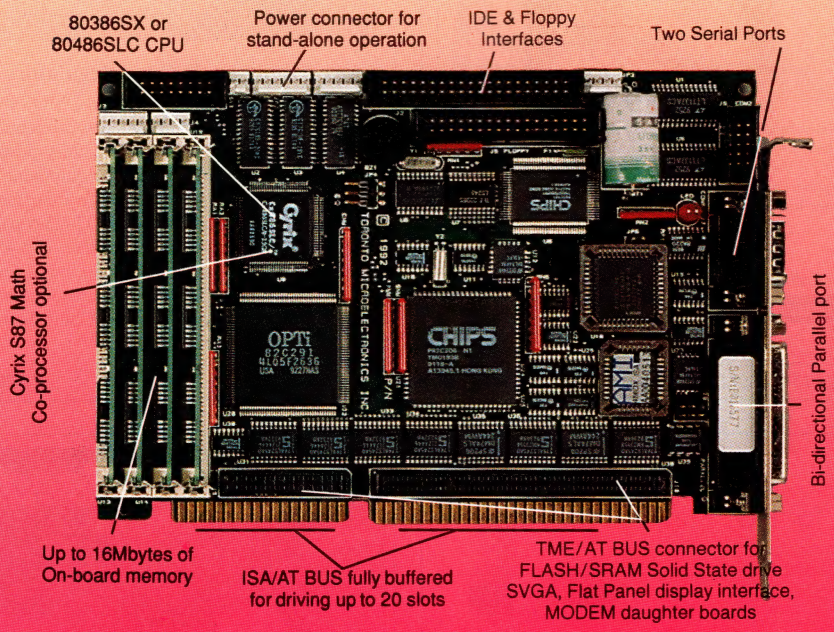
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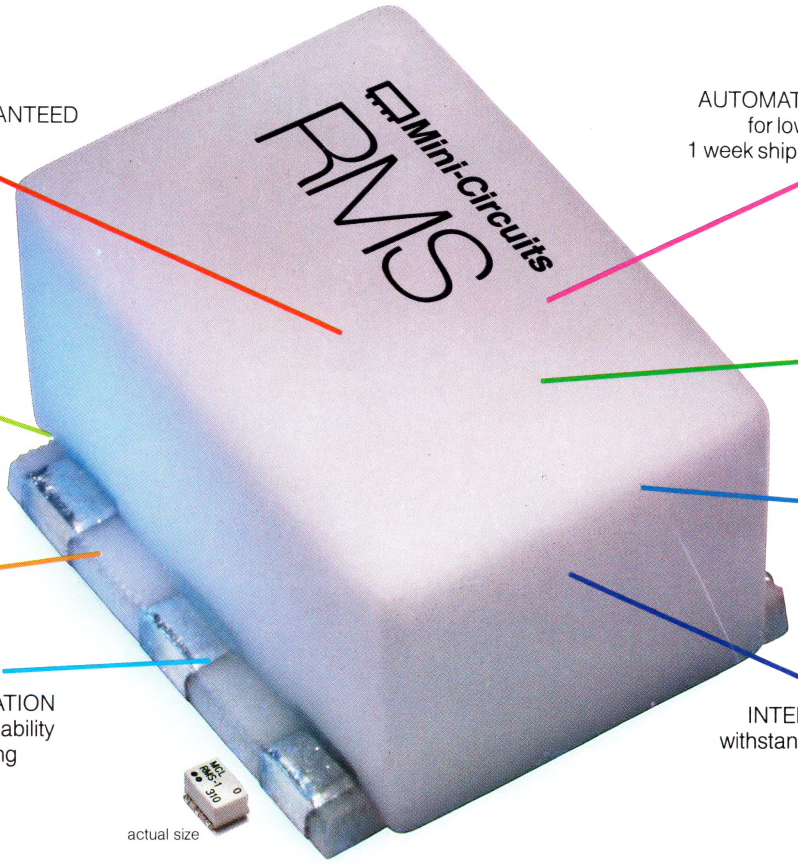

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